Design and Integration of a Single-chip 1-V CMOS IEEE 802.11a Transceiver

by

Leung Lai Kan

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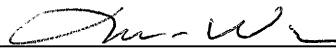

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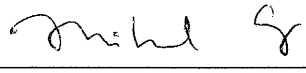

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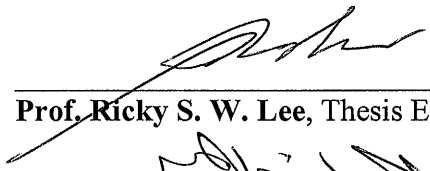

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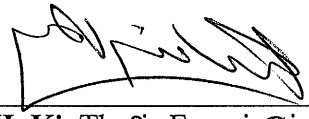

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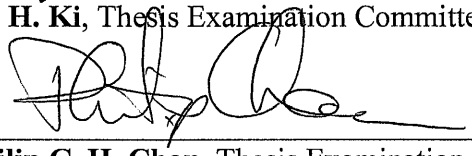

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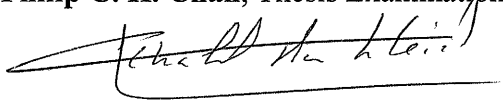

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Design and Integration of a Single-chip 1-V CMOS IEEE 802.11a Transceiver

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Abstract

Wireless local area network systems have received much attention in recent years. The market of wireless LAN systems has been booming so fast that the demand for low-cost, low-power and high-performance WLAN transceivers has grown dramatically.

In this dissertation, a 1-V CMOS frequency synthesizer for IEEE 802.11a is proposed by using a transformer-feedback VCO for low voltage and a stacked divider for low power. The novel design makes use of on-chip transformer and no other off-chip component is necessary. Implemented in 0.18μm CMOS process, the frequency synthesizer is operated with a 1V supply while consuming only 10mW and occupying an area of 1.28mm^2. It measures a phase noise of -139dBc/Hz at an offset of 20MHz with a center frequency of 4.256GHz.

To further improve the performance of VCOs and frequency synthesizers in terms of tuning range, a novel technique to implement an integrated variable inductor using an on-chip transformer is also proposed. The design principle and optimization techniques are investigated. Employing such a variable inductor, a VCO is

demonstrated to oscillate in 2 distinct frequency bands from 2.2GHz to 3.6GHz and from 10.7GHz to 11.3GHz. It consumes only 5mW with a 1V supply while occupying an area of 0.32mm^2.

A 1-V CMOS IEEE 802.11a WLAN transceiver is also proposed. The aforementioned frequency synthesizer is integrated into the transceiver onto the same chip. The transceiver uses a zero-IF, dual-conversion topology. The receiving path includes all the building blocks from the LNA to the ADC and the transmitting path includes all the building blocks from the DAC to the PA. Fabricated in 0.18-μm CMOS process and operated at a single 1V supply, the receiver and the transmitter consume 85.7mW and 53.2mW, both including the frequency synthesizer. The total chip area with pads is 12.5 mm^2.

Chapter 1 Introduction

1.1 Demand for transceivers

Wired local area networks in many different forms, had been dominating for decades since the internet revolution. However, with the ever increasing demand for mobile internet connectivity for real-time information access in locations such as airports, hotels and hospitals, wireless technology is getting much more attention. The use of wireless LAN removes the need to pull cable through walls and ceilings, increasing the installation speed and flexibility and reducing the implementation cost.

In the early generation of the wireless technology, WLAN is originally employed as an alternative for interconnections between desktops or notebook computers within residential apartments or offices. Now, WLAN networks are being applied as high-speed and broadband connections between mobile devices, like handsets, handheld PC and even digital cameras and camcorders. Sales of these consumer electronics with embedded WLAN have been booming since 2004 and will continue to prosper rapidly, as shown in Fig. 1.1. This commercial factor increases the demand for the design of high-performance WLAN transceiver with low-power consumption, small chip area and low cost.

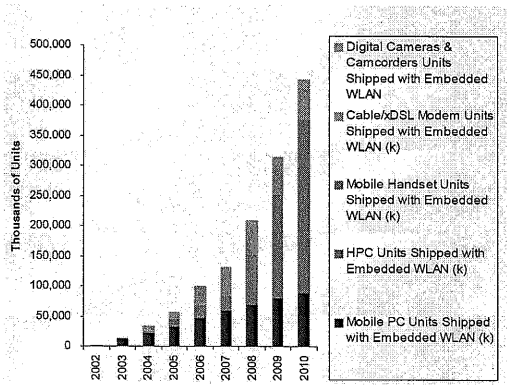


Fig. 1.1 Market sales of mobile devices embedded with WLAN [1]

1.2 Limitations of existing solutions

A summary of some existing WLAN transceivers is listed in Table 1.1.

		Vassiliou, I., et.al.[2]	Pengfei Zhang, et.al.[3]	T. Schwanenberger, et.al. [4]	T. Maeda, et.al. [5]
Process		1P6M CMOS 0.18μm	1P6M CMOS 0.18μm	BiCMOS SiGe 0.5μm	1P6M CMOS 0.18μm
Supply Voltage		1.8V	1.8V	1.9V	1.8V
Power	TX+Synthesizer	302mW	171mW	306mW	108mW
	RX+Synthesizer	248mW	135mW	321mW	118mW
Area		18.5mm^2	13mm^2	17mm^2	17.2 mm^2
Including IQ ADCs and DACs ?		No	No	No	No

Table 1.1 Summary of some existing WLAN transceivers

All of the above existing WLAN transceivers operate with supply voltage of, at least, 1.8V. They are power hungry, with power consumption more than several hundred milli-watts while occupying chip area much larger than 13mm^2. This increases the cost, sizes and complexity of the final products. Given the demand for portable devices embedded with WLAN, as shown in Fig. 1.1, a CMOS WLAN transceiver with much lower power consumption (<200mW), lower supply voltage (1V) and smaller chip area (<13mm^2) is proposed. The frequency synthesizer, power amplifier as well as the ADC and DAC are all integrated on the same chip.

1.3 Challenges of the proposed solution

1.3.1 CMOS technology

BiCMOS and GaAs technologies had been very more popular for RF applications than CMOS process. One of the major reasons is the relatively lower speed of CMOS devices. However, with the vast development in CMOS technology in recent years, its unity-gain frequency, which is an important figure of merit for RF performance, improves in a great amount. Fig. 1.2 shows the trend of the unity-gain frequency as a function of gate length in CMOS technology. Even for the commonly

available 0.18□m process, its unity-gain frequency is around 60GHz, which is well sufficient for applications at 5GHz.

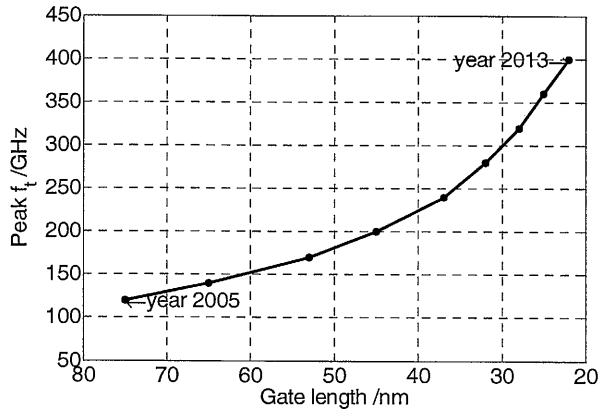


Fig. 1.2 Peak ft as a function of gate length [6]

Yet, drawbacks, such as the short-channel effect and the relatively lower quality factor of passive components in CMOS technology, remain unfavorable for RF applications. Special structures and circuit techniques will be applied in this dissertation to address these problems.

1.3.2 Low power consumption

The aforementioned portable consumer electronics call for usage for long periods of time. Enhancing the battery life is one approach to increase the usage time. However, due to limited improvement in the battery industry, low-power design techniques are more effective to make efficient use of energy in these portable devices for anywhere and anytime internet connections.

Low power consumption also reduces the operating temperature of the chip. This helps to remedy problems, such as electrical parameter shift. Packages can be much smaller by reducing or even eliminating the heat sinks. All these imply smaller dimensions and much longer lifetime for the devices.

The proposed transceiver is to dissipate less than 200mW. Innovative circuit designs are required for proper operation with this level of power consumption.

1.3.3 Low supply voltage

The power consumption of a digital integrated circuit can be estimated using the following equation,

$$P = fC_{load}V_{dd}^{2} + I_{leak}V_{dd} + I_{short}V_{dd} \quad (1)$$

where f is the operating frequency of the circuit, C_{load} is the loading capacitance, I_{leak} is the leakage current and I_{short} is the short-circuit current

It is obvious from the above equation that the most effective way to lower the power consumption in digital circuits is to reduce the supply voltage. However, this may not be applied to analog circuits. Reducing the supply voltage for an analog circuit usually reduces its signal-to-noise ratio. Bias currents have to be increased to keep the original signal-to-noise ratio. As a result, power consumption may not be reduced. Even if it is, the reduction is less significant than that in the digital circuits.

Yet, it is still desirable to use the same low-supply voltage for both analog and digital circuitry. Because in a transceiver, power dissipated by the digital circuits usually dominates the total values. Reducing the supply voltage is still beneficial to the transceiver as a whole. Moreover, by using the same level of supply voltage, no extra voltage multiplier or DC-to-DC boost converter is required for the analog circuits. This minimizes the complexity of the transceiver.

Gate length continues to scale down as the need for high-speed circuits and highly packed devices increases. Lowering the supply voltage is inevitable to avoid oxide breakdown. The trend of CMOS supply voltage as a function of gate length is shown in Fig. 1.3. For 0.18□m technology, the nominal supply voltage is reduced to

1.8V. In the proposed transceiver, a 1V supply voltage is used. This is around 55% of the nominal value.

However, threshold voltage of the CMOS device does not follow the drop in the supply voltage to avoid excessive leakage current. The available voltage headroom is limited for low-supply voltage operation. This may result in smaller voltage gain, poorer linearity and etc. Again, innovative circuit techniques are required to overcome these problems.

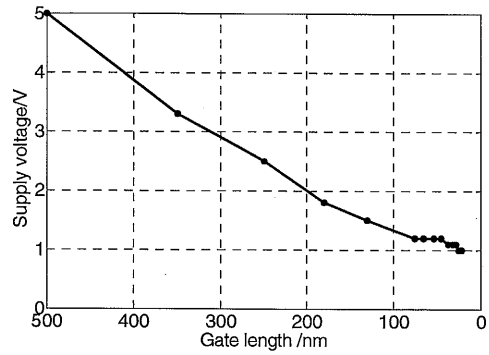


Fig. 1.3 Supply voltage as a function of gate length [6]

1.3.4 Level of integration

The highly packing property and the ability to integrate large high-speed digital blocks are attractive factors for using CMOS technology. In order to make use of such favorable factors, the mixed-signal building blocks, analog-to-digital converter and digital-to-analog converter, are integrated onto the same chip with the analog part of the RF transceiver. This helps to reduce the parasitics in the input and output interface of different building blocks, which implies better performance, lower complexity and production cost. However, this requires careful floor-planning of the digital and analog circuitry.

1.4 Organization of this dissertation

This dissertation is divided into 8 chapters. Following this chapter, the background and specifications of the IEEE 802.11a standard are addressed in Chapter 2. In Chapter 3, different architectures are briefly described and compared. The architecture and specifications for the proposed transceiver are discussed in this chapter. The design of the frequency synthesizer is described in Chapter 4. This will be followed by the detailed analysis and discussion on further development of the VCO in Chapter 5. The design and implementation of other building blocks in the proposed transceiver are described in Chapter 6. Measurement results of the proposed transceiver are presented in Chapter 7. Conclusions and further improvement of the proposed transceiver are discussed in Chapter 8.

Chapter 2 Background

2.1 IEEE 802.11a WLAN communication system

2.1.1 Overview

The IEEE 802.11 standard family, also called the Wi-Fi standard, is the most commonly used set of WLAN standards. The standards are meant to extend wired Ethernet to the wireless domain. There are at least 8 such standards available in the family with more to come in the near future.

IEEE 802.11b and 802.11g are two of the standards, operating in the 2.4GHz frequency range. IEEE 802.11a is another example. It operates in a newly allocated unlicensed radio band, the 5-6GHz Unlicensed National Information Infrastructure (U-NII) band. The orthogonal frequency division multiplexing encoding scheme is used in this standard. The maximum distance covered is around 50m.

IEEE 802.11a provides greater bandwidth and more non-overlapping channels. Since it operates in the 5GHz frequency spectrum, it has less potential interference from cordless phones, Bluetooth devices and even microwave ovens than IEEE 802.11b and 802.11g. These advantages are particularly critical to recent applications like voice-over-WLAN, also called VoWLAN. It combines the network cost savings of Wi-Fi with the voice efficiency of voice-over-IP, also known as VoIP. These phone calls are clearer than cell phone calls and are a lot less expensive. Because IEEE 802.11b and 802.11g have only three non-overlapping channels, they only support 6-8 calls simultaneously. In contrast, IEEE 802.11a has 12 non-overlapping channels. It is able to handle 15-20 voice-over-IP calls from a single WLAN access point.

2.1.2 OFDM system

IEEE 802.11a uses a multi-carrier modulation scheme, orthogonal frequency division multiplexing, also called OFDM. The basic idea of OFDM is to transmit information using a number of narrow-band subcarriers instead of a single wide-band carrier.

The orthogonal carriers, which allow for spectrum overlapping, help to eliminate the inter-carrier guard bands between the carrier and saves much bandwidth when compared to normal FDM signal. This implies an increase in the spectral efficiency for OFDM system. Apart from the above advantage, OFDM is more resistant to frequency selective fading than single carrier systems because the channel is divided into narrowband flat fading sub-channels. In addition, channel coding and interleaving can be utilized to recover symbol lost due to the frequency selectivity of the channel. By using a cyclic prefix, inter-symbol interference (ISI) and inter-frame interference (IFI) can be eliminated. OFDM also facilitates simpler channel equalization than adaptive equalization techniques with single carrier systems.

Yet, OFDM is sensitive to synchronization. This requires the baseband in the receiver to perform synchronization task to determine the symbol boundaries are and optimal timing instants. Correction of the carrier frequency offset of the received signal is also needed. Another disadvantage is the high peak-to-average ratio of the OFDM signals. This requires high linearity performance in the transceiver. The block diagram of the transmitter and receiver for the OFDM physical layer is shown in Fig. 2.1.

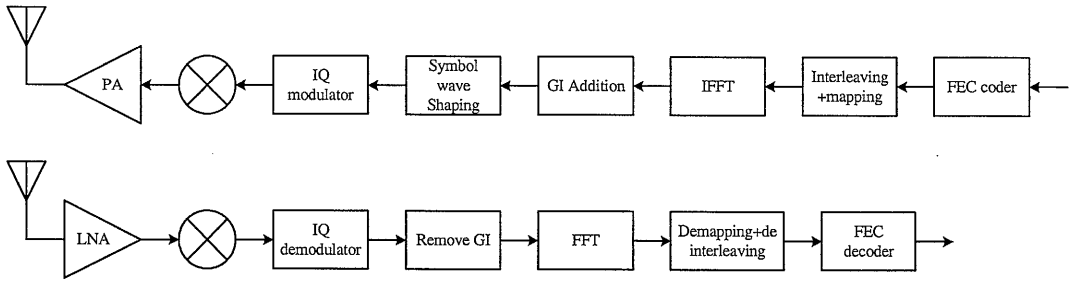


Fig. 2.1 Block diagram of the transmitter and receiver for the OFDM physical layer

Each user uses all the sub-carriers simultaneously to transmit the data. The access technique used is frequency-division multiple access (FDMA). The duplex method used is time-division duplex (TDD) under which a single frequency channel is used for both uplink and downlink with different time slots.

2.1.3 Specification of the physical layer of IEEE 802.11a [7]

2.1.3.1 Frequency allocation

As mentioned previously, IEEE 802.11a operates in the U-NII band, from 5-6GHz. A total bandwidth of 300MHz is allocated. It is divided into three frequency bands, as shown in

Fig. 2.2. The lower band, middle band and upper band occupied the frequency spectrum from 5.15-5.25GHz, 5.25-5.35GHz and 5.725-5.825GHz respectively. Each band occupies a bandwidth of 100MHz, containing four channels with bandwidth of 20MHz. A total of 12 non-overlapping channels are provided, 8 dedicated to indoor and 4 to point to point communication.

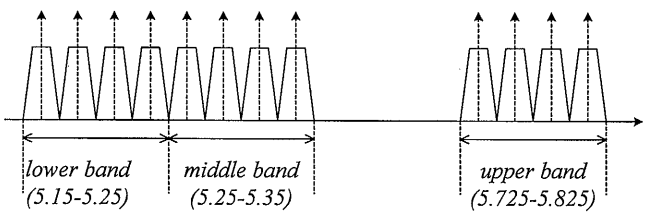


Fig. 2.2 Three frequency bands in IEEE WLAN 802.11a

2.1.3.2 Frequency channel

Each channel is sampled at 20MHz using OFDM transmission scheme. Within each channel, there are 64 subcarriers. 12 of them are zero subcarriers. 48 are data subcarriers and 4 are pilot subcarriers for synchronization tracking. A simplified diagram representing the subcarriers in each frequency channel is shown in Fig. 2.3. The subcarriers are spaced, 20MHz/64=312.5kHz, apart. This corresponds to an equivalent symbol period of 3.2μs. Since the OFDM symbol duration is 4μs, the duration of the guard interval is 800ns. As mentioned before, because twelve of the sub-carriers are zero carriers, the occupied bandwidth is only 16.6MHz.

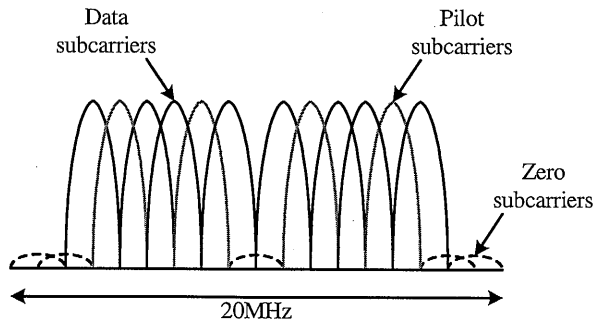


Fig. 2.3 Sub-carriers in each frequency channel

Among the zero subcarriers, the one located at DC, as shown in Fig. 2.4, is the most important. As mentioned previously, in order to avoid difficulties in the digital-to-analog and analog-to-digital converter, offsets and carrier feedthrough in the RF system, the subcarrier falling at DC, also called the zeroth subcarrier, is not used. Since the bandwidth of the subcarrier is 312.5kHz, there is an empty spectrum of ±156.25kHz, centered at the zero frequency. If the spectrum is transmitted through a high-pass filter with a corner frequency below 156.25kHz, the DC components, which poses problems like DC offsets and carrier feedthrough, of the channel can be filtered out, without affecting the carrying information.

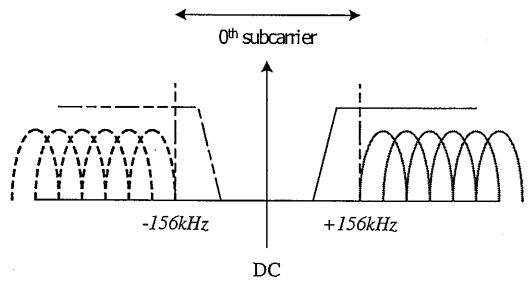


Fig. 2.4 The zeroth subcarrier

2.1.3.3 Data rate

Flexible data rates, from 6Mb/s to 54Mb/s, are supported in the standard for transmission covering different distances. The specified data rate under different modes of modulation is listed in Table 2.1. The modulation schemes include BPSK, QPSK, 16-QAM and 64-QAM. The maximum data rate allowed is 54Mb/s using 64-QAM with a coding rate of 3/4.

Data rate /Mb/s	Modulation	Coding rate
6	BPSK	1/2
9	BPSK	3/4
12	QPSK	1/2
18	QPSK	3/4
24	16-QAM	1/2
36	16-QAM	3/4
48	64-QAM	2/3
54	64-QAM	3/4

Table 2.1 Data rates for different modulations and coding rates

2.1.3.4 Output power of the transmitter

The maximum allowable output power according to FCC regulations is listed in Table 2.2. The maximum output power allowed is 800mW, which is equivalent to 29dBm.

Frequency band /GHz	Maximum output power
UN-II lower band: 5.15-5.25	40mW (2.5mW/MHz)
UN-II middle band: 5.25-5.35	200mW (12.5mW/MHz)
UN-II upper band: 5.725-5.825	800mW(50mW/MHz)

Table 2.2 Maximum allowable output power

2.1.3.5 Input power of the receiver

The minimum input level sensitivity of the receiver for different data rates is listed in Table 2.3. The maximum input power shall not exceed -30dBm.

Data Rate /Mb/s	Minimum sensitivity /dBm
6	–82
9	–81
12	–79
18	–77
24	–74
36	–70
48	–66
54	–65

Table 2.3 Specified minimum input level sensitivity for different data rates

2.1.3.6 Packet error rate

PER is a measure of the noise performance of a system. It defines the noise figure and the sensitivity of a receiver. In IEEE 802.11a, the receiver is required to have a packet error rate less than 10% at a *PHY sub-layer service data unit* (PSDU) length of 1000 bytes for all the modulation and data rates.

2.1.3.7 Transmitter constellation error

The relative constellation RMS error is also expressed as error vector magnitude (EVM) in a unit, %rms. The value is averaged over subcarriers, OFDM frames and packets. The specified relative constellation error and EVM for different data rate is shown in Table 2.4.

Data rate /Mbits/s	Relative constellation error /dB	EVM %
6	–5	56.234
9	–8	39.811
12	–10	31.623
18	–13	22.387
24	–16	15.849
36	–19	11.220
48	–22	7.943
54	–25	5.623

Table 2.4 EVM specification for different data rates

All the above specifications are summarized in Table 2.5.

Frequency Bands	5.15-5.35GHz 5.725-5.825GHz
No. of Channels	12
Channel bandwidth	20MHz
Multiple access method	CSMA/CA
Duplex Method	TDD
Users per channel	127
Modulation	OFDM with BPSK, QPSK, 16-QAM, 64-QAM
Data rate	6-54Mb/s
PER	<10%
Transmitter relative constellation error	-5@6Mb/s -25dB@54Mb/s
Output power	40mW (lower band) 200mW (middle band) 800mW(upper band)
Sensitivity	-82dBm (for 6Mb/s) -65dBm (for 54Mb/s)
Max. input signal	-30dBm (for 54Mb/s)

Table 2.5 Summary of specifications for IEEE 802.11a standard

2.2 Fundamental figure of merits for transceivers

2.2.1 Conversion gain

It is the ratio of the output voltage or power to the input signal of a device, usually expressed in dB. The input and output frequency may not be the same. It is a measure of the amplifying capability of the device. Voltage and power gain of each building block has to be considered in different scenarios and should be inter-changeable. The conversion from voltage gain to power gain involves the input and output impedances of the previous and subsequent stages, as shown in Fig. 2.5. Their relationship can be written as [8],

$$A_{p,n} = \left(\frac{R_{in,n}}{R_{out,n-1} + R_{in,n}} \right)^2 A_{v,n}{}^2 \frac{R_{out,n-1}}{R_{out,n}} \qquad (2.1)$$

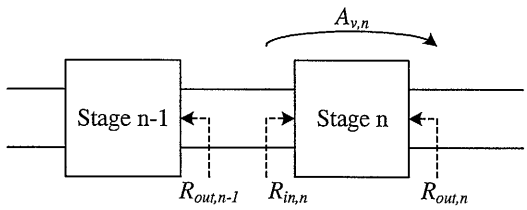


Fig. 2.5 Conversion of voltage gain to conversion gain between cascaded stages

In CMOS technology, input is usually applied to the gate of the MOS. Impedance of the gate input is usually capacitive. For channel-selection filter, VGA and ADC, the operating frequency is low and the input impedance can usually be assumed to be large. Yet, for LNA and down-conversion mixer, the operating frequency is as high as 5GHz. Capacitive loading is very critical to the performance of these building blocks and should be determined carefully.

The cascaded conversion gain of a receiver or transmitter is the sum of the voltage or power gain of all the building blocks.

2.2.2 Noise figure

Noise factor is the ratio of the ratio of the total output noise power to the output noise due to the input source only. The following equation is used to derive the noise figure in dB of a receiver,

$$\begin{aligned} NF &= 10\log\left(\frac{n_{out,total}}{n_{out,insrc}}\right) \\ &= n_{out,total} - n_{in} - Gain \end{aligned} \tag{2.2}$$

where $n_{out,total}$ is the total output noise power density, $n_{out,insrc}$ is the output noise power density due to the input source only and n_{in} is the input noise power density

The input noise power density can be written as,

$$n_{in} = kT \tag{2.3}$$

where k is the Boltzmann's Constant (1.38×10^{-23}J/K) and T is the temperature in Kelvin

Noise power density is measured in *dBm/Hz*. It can be expressed as,

$$dBm/Hz = 10\log\left(\frac{Power\ density\ per\ Hz\ (W/Hz)}{1mW}\right) \tag{2.4}$$

At room temperature, 300K, the value of n_{in} is -174dBm/Hz and the equation for calculating noise figure can be simplified as,

$$NF = n_{out,total} - Gain - 174dBm/Hz \tag{2.5}$$

The cascaded noise figure of a receiver [8] can be expressed as,

$$NF_{total} = NF_{@R_{50\Omega,LNA}} + \frac{\left(NF_{@R_{out,mixer}} - 1\right)}{A_{p,LNA}} + \frac{\left(NF_{@R_{out,filter}} - 1\right)}{A_{p,LNA}\cdot A_{p,mixer}} + \frac{\left(NF_{@R_{out,VGA}} - 1\right)}{A_{p,LNA}\cdot A_{p,mixer}\cdot A_{p,filter}} \tag{2.6}$$

where $NF_{@R_{out,n-1}} = NF_{@50\Omega}\times\frac{50}{R_{out,n-1}}$

It is obvious from the above equation that the cascaded noise figure of a receiver is dominated by the individual noise figure and power gain of the LNA. The contribution of the following building blocks diminished as a consequence of the positive power gain introduced by the previous stages.

2.2.3 Signal-to-noise ratio

Output signal-to-noise ratio is another important parameter to define the performance of a receiver. It is a ratio of the desired output signal power to the noise floor, which can be written mathematically as,

$$SNR_{out}(dB) = Output\ signal\ power\ (dBm) - noise\ (dBm) \tag{2.7}$$

However, in IEEE 802.11a, the required output SNR is not specified in the standard. Instead, packet error rate (PER) is used to specify the noise performance of the receiver. It is expressed in %, defining the percentage of packets received incorrectly for a number of packets transmitted. Since it is complicated for circuit simulator to obtain such parameter, it is first converted to bit error rate (BER), which can be used to derive the required output SNR. It is worth noting that the required BER depends on the type of modulation used. Detail about the derivation of the specified SNR is to be discussed in the next chapter.

2.2.4 Linearity

A commonly used figure of merit used for characterizing the linearity performance of an OFDM system is the out-of-channel input-referred third order intercept point. It is usually expressed in *dBV* or *dBm*. The conversion of *dBm* to *dBV* can be expressed as,

$$\begin{aligned} dBm &= 10\log\left(\frac{V_{rms}^{\ 2}}{50}/1mW\right) \\ &= 20\log(V_{rms})+13 \\ &= dBV+13 \end{aligned} \tag{2.8}$$

For the out-of-channel IIP3, the two interferers are assumed to originate outside the 20MHz channel. For example, it is assumed that the two interferers are located at 5.275GHz and 5.295GHz, as shown in Fig. 2.6. They are 20MHz and 40MHz away from the desired center frequency of the RF channel, which is 5.255GHz under such scenario. The two interferers are down-converted to 25MHz and 45MHz respectively and generate a 5MHz intermodulation product, which is in-band, in-channel and located at the center of the IF channel. By sweeping the RF input power of the

interferers, the relation between the input and output power of the interferers and the intermodulation products can be measured.

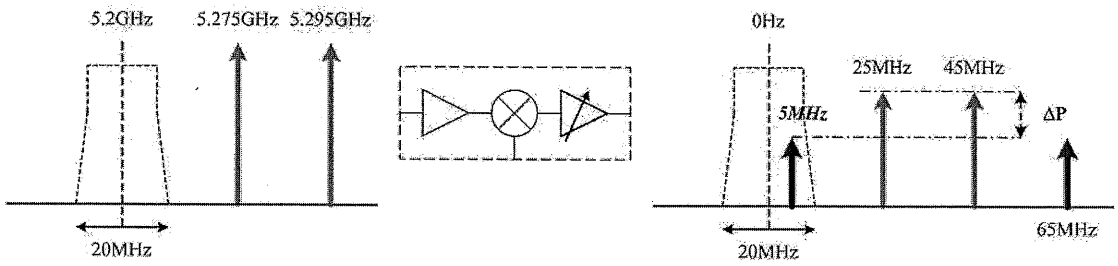


Fig. 2.6 Input and output signals for testing out-of-band IIP3 in the receiver

The IIP3 can be calculated directly by using the equation below,

$$IIP3 = P_{in} + \frac{\Delta P}{2} \tag{2.9}$$

where P_{in} is the input power to the receiver and ΔP is the difference between the intermodulation product and the fundamental

P_{in} in the equation above has to be sufficiently small to ensure that the receiver is free from any distortion but large enough to generate IM3 larger than the output noise floor. Otherwise, the IIP3 calculated will be incorrect.

The graphical approach to obtain the IIP3 is a more tedious method. However, it ensures that the above issue about the distortion on the input signal is taken into account. The principal idea is to plot the desired fundamental output and the third order intermodulation products obtained previously as a function of the RF input power onto the same graph. The third-order intercepting point is the extrapolated intersection of such two curves, as shown in Fig. 2.7.

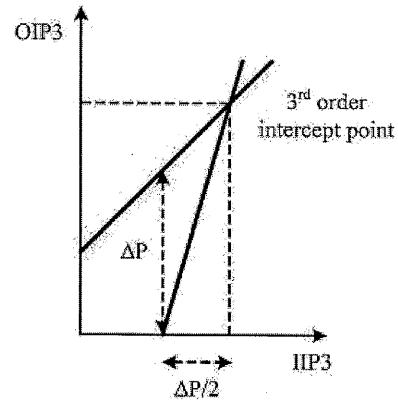


Fig. 2.7 Graphical approach to calculate the IP3 of a system

The cascaded linearity of the receiver [8] can be written as,

$$\frac{1}{IP3_{total}^{\ 2}} = \frac{1}{IP3_{LNA}^{\ 2}} + \frac{A_{v,LNA}^{\ 2}}{IP3_{mixer}^{\ 2}} + \frac{A_{v,LNA}^{\ 2} A_{v,mixer}^{\ 2}}{IP3_{filter}^{\ 2}} + \frac{A_{v,LNA}^{\ 2} A_{v,mixer}^{\ 2} A_{v,filter}^{\ 2}}{IP3_{VGA}^{\ 2}} \tag{2.10}$$

The IM3 product, acting as an in-band interferer, can be reduced by minimizing the third-order IM contribution from the channel-selection filter and the variable gain amplifier. This is done by introducing a certain amount of IF selectivity to these out-of-channel interferers in the mixer and the channel-selection filter. IF selectivity refers to the attenuation relative to the pass-band conversion gain, at the frequency in the stop-band where the out-of-channel interferers locate. The IF selectivity reduces the third-order distortion of the subsequent building blocks. By including such selectivity into the cascaded linearity of a receiver, the above equation can be rewritten as,

$$\frac{1}{IP3_{total}^{\ 2}} = \frac{1}{IP3_{LNA}^{\ 2}} + \frac{A_{v,LNA}^{\ 2}}{IP3_{mixer}^{\ 2}} + \frac{A_{v,LNA}^{\ 2} A_{v,mixer}^{\ 2}}{IP3_{filter}^{\ 2} L_{mixer}^{\ 2}} + \frac{A_{v,LNA}^{\ 2} A_{v,mixer}^{\ 2} A_{v,filter}^{\ 2}}{IP3_{VGA}^{\ 2} L_{filter}^{\ 2}} \tag{2.11}$$

where L_{mixer} and L_{filter} is the selectivity of the down-conversion mixer and the channel-selection filter in the stop-band

By introducing appropriate selectivity, the third and fourth terms of the equation can be neglected. The linearity of the receiver is, thus, dominated by the conversion gain of the LNA and the linearity of the down-conversion mixer.

The 1dB compression point, also written as P_{1dB}, is another measure of the linearity of a system. It indicates the point where the gain of a system is compressed by 1 dB, compared to the ideal linear gain curve. Typically, assuming that a device has a flat frequency response, the 1dB compression point is about 10 to 15 dB below the third-order intercept point.

2.2.5 Error vector magnitude

Error vector magnitude (EVM) is a figure of merit of modulation accuracy used to quantify the performance of the transmitter under the influence of non-idealities such as nonlinear distortion. Error vector is the difference between an ideal modulation vector and the actual modulation vector, as shown in Fig. 2.8. EVM is the square root of the ratio of the mean error vector power to the mean reference power. It can be calculated by using the following equation,

$$EVM = \sqrt{\frac{mean\ error\ vector\ power}{mean\ reference\ power}} \times 100\% \qquad (2.12)$$

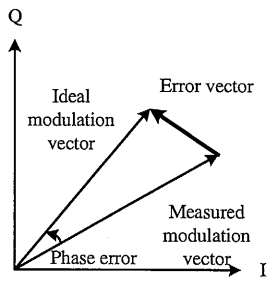


Fig. 2.8 Graphical representation of EVM

In IEEE 802.11a, EVM_{rms} is used to characterize the transmit modulation accuracy. It is expressed mathematically as,

$$EVM_{rms} = \frac{\sum_{i=1}^{N_f} \sqrt{\frac{\sum_{j=1}^{L_p}\left[\sum_{k=1}^{52}\left\{(I(i,j,k)-I_0(i,j,k))^2+(Q(i,j,k)-Q_0(i,j,k))^2\right\}\right]}{52L_p \times P_0}}}{N_f} \quad (2.13)$$

where L_p is the length of the packet, N_f is the number of frames for the measurement, $(I_0(i,j,k), Q_0(i,j,k))$ is the ideal symbol point of the ith frame, jth OFDM symbol of the frame, kth subcarrier of the OFDM symbol in the complex plane, $(I(i,j,k), Q(i,j,k))$ is the measured symbol point of the ith frame, jth OFDM symbol of the frame, kth subcarrier of the OFDM symbol in the complex plane, P_0 is the average power of the constellation

EVM_{rms} can be expressed in either dB or %. The conversion is done by using the following equation,

$$\begin{aligned} \%_{EVM} &= 10^{\left(\frac{dB_{EVM}}{20}\right)} \\ dB_{EVM} &= 20\log_{10}(\%_{EVM}) \end{aligned} \quad (2.14)$$

2.2.6 IQ imbalance and sideband rejection

IQ imbalance is another key parameter to the performance of OFDM system. It comprises of gain and phase imbalance and reflects the circuit mismatches in the quadrature paths of a system. It is one of the circuit impairments which affect the values of constellation error or error vector magnitude specified in the standard. Its requirement varies with different types of modulation.

The sideband rejection is also closely related to the IQ imbalance of a system. It is a ratio, usually expressed in *dBc*, of the desired output power and the sideband power. It can be mathematically translated to amplitude and phase mismatch as,

$$SBR = 10\log\left(\frac{A_{IQ} + \frac{1}{A_{IQ}} + 2\cos(\theta)}{A_{IQ} + \frac{1}{A_{IQ}} - 2\cos(\theta)}\right) \tag{2.15}$$

where $A_{IQ} = \frac{A_I}{A_Q}$ and $\theta = \frac{(\theta_I - \theta_Q)\pi}{180}$

2.2.7 Phase noise

Phase noise is a measure of the spectral purity of an oscillator. It is defined as the ratio of the single sided spectral noise density to the carrier power at a particular offset from the center frequency. It can be mathematically written as,

$$L\{\Delta\omega\} = 10\log\left(\frac{noise\ power\ in\ a\ 1Hz\ bandwidth\ at\ frequency\ \omega_0 + \Delta\omega}{carrier\ power}\right) \tag{2.16}$$

It can be calculated by measuring the noise power within a unit bandwidth at an offset Δω from the carrier and divide it by the carrier power, as shown in Fig. 2.9.

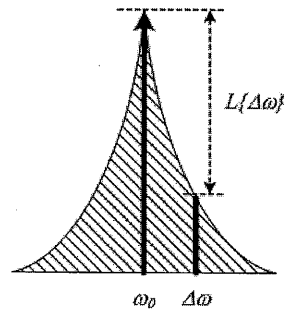


Fig. 2.9 Graphical representation of phase noise

Phase noise originates from random noise in the reference input, PFD, loop filter and the VCO. Phase noise in the LO signals generated by the frequency synthesizer can degrade the sensitivity of a receiver due to reciprocal mixing[9], as shown in Fig. 2.10. Apart from the wanted signal, interferers and some other unwanted signal are present at the input of a receiver. When they are all

down-converted to the IF frequency by the LO signal with phase noise, the wanted signal may be corrupted by the phase noise imposed on the unwanted signal if the phase noise is too bad. Therefore, it is critical to meet the specified phase noise in designing the frequency synthesizer.

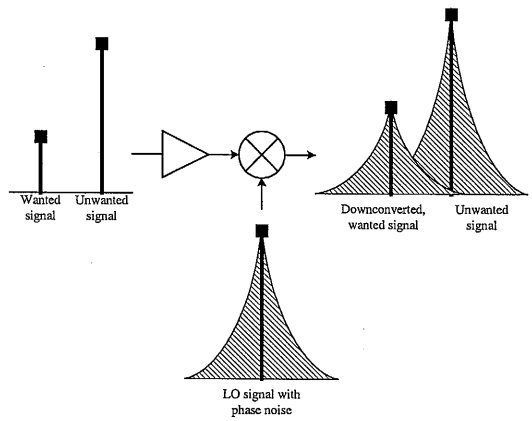


Fig. 2.10 Reciprocal mixing

Chapter 3 Architecture and specification of the proposed transceiver

3.1 Overview of transceiver architectures

Different topologies available for design of transceivers are reviewed. Common architectures include conventional super-heterodyne and direct-conversion topologies. A zero-IF and dual conversion topology, arising great attention in recent years, is also investigated.

3.1.1 Super-heterodyne topology

A receiver utilizing super-heterodyne topology is shown in Fig. 3.1.

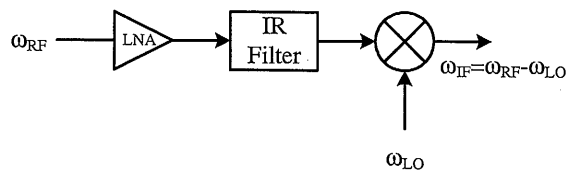


Fig. 3.1 A super-heterodyne receiver

The fact that ω_{IF} is much lower than ω_{RF} helps to relax the qualify factor of the channel-select filter. Moreover, since ω_{RF} is different from ω_{LO}, even if LO leakage exists, it does not induce any self-mixing and poses no DC offset. Offset cancellation mechanism is, thus, not important in such topology. Similarly, even if the PA output is coupled to the VCO, frequency pulling is not likely to happen in the VCO.

Yet, the image at a frequency of $\omega_{image} = 2\omega_{LO} - \omega_{RF}$ is also down-converted to the IF output and corrupts the desired signal unless it is suppressed by an image-reject filter placed after the LNA, as shown in Fig. 3.2. Such IR filter is very

difficult to be implemented on chip because it is required to have small loss in the desired band and a large attenuation in the image band.

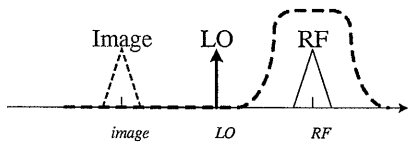


Fig. 3.2 Image filtering in a super-heterodyne receiver

One approach to relax the requirement of the IF filter in the super-heterodyne topology is to use image rejection architecture such as Hartley and Weaver architectures, in which additional quadrature mixing and phase-shifting is required. The image rejection attained is sensitive to the amplitude and phase imbalance between the quadrature paths in these architectures. Therefore, the typical image rejection yielded by these techniques is about 40dB, which is still not high enough to maintain good signal quality for a super-heterodyne receiver. The super-heterodyne topology is still not a good single-chip solution.

3.1.2 Direct-conversion topology

One way to remove the image filtering problem is to use a direct-conversion topology. A direct-conversion receiver front-end is shown in Fig. 3.3. A simple low-pass filter is sufficient for the channel selection at the output of the mixer. No image signal is present in such topology.

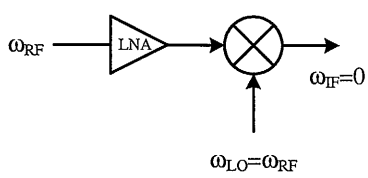


Fig. 3.3 A direct-conversion receiver

Because the positive and negative part of the input spectrum overlaps with each other in the direct-conversion topology, it is important to use quadrature paths for frequency and phase modulated signal to avoid loss of information.

The reasons why direct-conversion architecture prevails is the elimination of image filter. Higher level of integration is therefore feasible. However, drawbacks of direct-conversion architectures are still great obstacles. Because the RF signal is at the same frequency as the LO signal, low-frequency flicker noise exists in the desired band and reduce the signal integrity. This is especially significant in CMOS devices owing to its higher flicker noise corner frequency than its counterparts. The high-level LO power is another issue in a direct-conversion receiver. When the LO power is strong enough to couple into the antenna, the RF front-end may be easily saturated and the same receiving band of other users will be corrupted. This is called *LO leakage*. It also induces *DC offsets* in the receiver. When the LO signal, which leaks to the RF front-end, reaches the down-conversion mixer, self-mixing in the mixer generates DC offsets. Mismatches in the mixer also induce DC offsets. DC offsets generated in the mixer is amplified and saturates the following stages, including the channel-selection filter, VGA and ADC. As a result, the sensitivity of the receiver is limited.

Other drawbacks of the direction-conversion transceiver includes frequency pulling, I/Q matching, even-order distortion, etc. All the above difficulties can be ameliorated, but usually at the expense of power consumption.

3.2 Existing solutions

[10] is a direct-conversion transceiver. The transceiver is a two-chip solution; one chip for RF transceiver and the other for BB processor. The frequency

synthesizer is also integrated into the RF transceiver. The oscillation frequency of the VCO used is half of the carrier frequency. The output of the VCO is multiplied by a frequency doubler before it is connected to the mixers in the transceiver. Its purpose is to avoid frequency pulling from the RF output from the transmitter. Both the ADC and DAC are included in the BB processor with the DSP. IQ mismatches and DC offsets in the RF transceiver is compensated using the DSP. The transceiver operates under 1.8V supply and consumes 302mW and 248mW for transmit and receive mode. The total chip area for the RF transceiver is 18.5mm^2.

[11] is also a direct-conversion transceiver. The VCO oscillates at 1.5 times lower than the desired RF frequency in order to minimize frequency pulling, LO leakage and DC offsets. A mixed-mode automatic frequency control is incorporated in the transceiver to remedy problems due to frequency offsets and multi-path distortion. A self-calibration mode is integrated to cancel the LO feedthrough and the image of the automatic frequency control (AFC) itself. The transceiver operates under 1.8V supply and consumes 171mW and 135mW for transmit and receive mode. It occupies an area of 13mm^2.

[12] is another direct-conversion transceiver. It includes the receiver, the transmitter, frequency synthesizer but not the ADC and DAC. The oscillation frequency of the VCO is twice that of the carrier frequency to avoid frequency pulling by the transmitter. The transceiver operates under 1.8V supply and consumes 108mW and 118mW for transmit and receive mode. It occupies an area of 17.2mm^2.

In summary, all the above transceivers operate under 1.8V supply and have power consumption more than several hundred milli-watts. The chip area occupied is also at least larger than 13mm^2. Since low supply voltage, low power consumption and small form-factor are all critical considerations for modern WLAN

battery-operated devices, a WLAN IEEE 802.11a single-chip transceiver with 1-V supply, power consumption around 100mW and chip area around 10mm^2 is proposed.

3.3 Proposed architecture of the transceiver

Recently, a zero-IF, dual-conversion transceiver architecture [13] is proposed. The frequency plan of the transceiver is shown in Fig. 3.4. It combines the features and advantages of the above architectures. After the LNA in the receiving path and before the PA in the transmitting path, two frequency conversions are utilized in the architecture. The input signal is first down-converted to a first IF at ω_{RF}-ω_{LO1}. The first IF signal is then down-converted by a second mixer with an LO signal at ω_{LO2}. After the two frequency conversions, the resultant IF is located at zero frequency. Quadrature paths are necessary, for the same reason as the direct-conversion topology. The purpose is to avoid loss of information for frequency and phase modulated input signals because the positive and negative part of the input spectrum overlaps with each other.

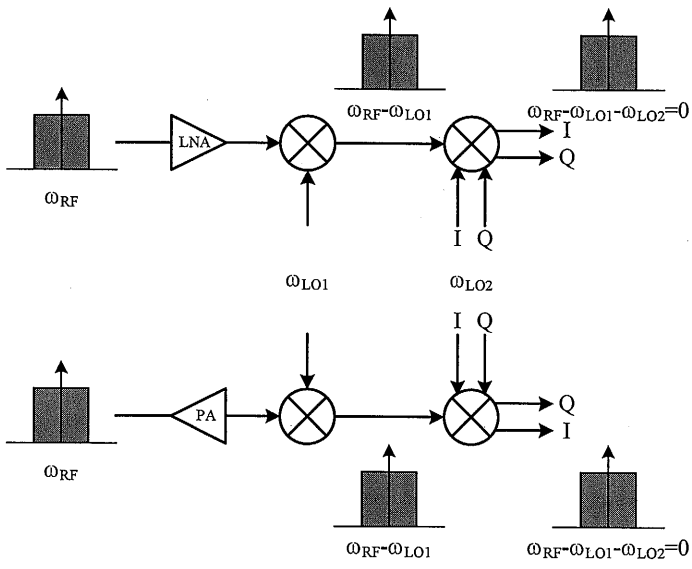


Fig. 3.4 Frequency plan in a zero-IF dual-conversion transceiver

The zero-IF, dual-conversion transceiver is a good candidate for single-chip solution not only because it eliminates the need for an image-reject filter but also because it has less problem with LO self-mixing and DC offset, low-frequency flicker noise. It needs no image-reject filter because the first IF, at ω_{RF}-ω_{LO1}, is relatively high. The image signal and the desired signal are very far apart. Because of the frequency selective characteristic of the LNA, the image signal can be easily attenuated before it is down-converted by the first mixer, as illustrated by Fig. 3.5.

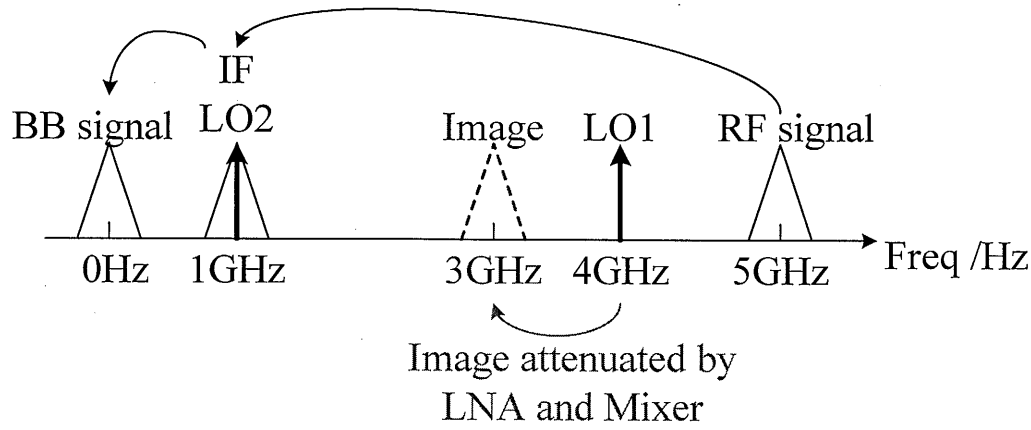


Fig. 3.5 Frequency conversion and image signal in a zero-IF dual-conversion transceiver

LO leakage, self-mixing and frequency pulling is not significant in this topology because the RF, first and second LO frequencies are totally different. Although the frequency of the inter-modulation product of the first and second LO signals is equal to the RF signal, the power level is much reduced. Also, The LOs generated by the frequency synthesizer has lower frequency than those in the direct-conversion topology. This can help to reduce the power consumption of the frequency synthesizer. By making use of a divider, a single frequency synthesizer is needed to generate the different LOs.

Because the resultant IF is placed at DC, problems due to DC offset and low frequency flicker noise still exist in such topology if nothing is applied to remedy this problem. But, fortunately, in an IEEE 802.11a system, in order to avoid difficulties in D/A and A/D converter offsets and carrier feedthrough in the RF system, the subcarrier falling at DC (the zeroth subcarrier) is not used. There is an empty spectrum of ±156.25kHz. If the corner frequency of a HPF falls below this value, the spectrum of the sub-channels carrying information will not be affected and the DC offsets and low-frequency flicker noise issues can be tackled.

The zero-IF and dual-conversion architecture, therefore, facilitates higher level of integration, lower power consumption and higher performance. Such dual-conversion topology calls for a frequency synthesizer that can generate 2 LO signals with the second LO_2 having in-phase and quadrature-phase outputs [13].

It is worth to note that direct-modulation technique is a possible topology for a transmitter. It requires only a frequency synthesizer and filters. However, it is not suitable for OFDM system like the IEEE 802.11a, which involves the transmission of non-constant envelope modulated signals.

Due to the above advantages, the architecture of the transceiver is chosen to be the zero-IF, dual-conversion topology. Differential configuration is applied through the whole transceiver because it is relatively immune to common-mode interference and noise. In addition, even-order distortion is not significant in differential devices. The architecture of the whole transceiver, including the frequency synthesizer, is shown in Fig. 3.6.

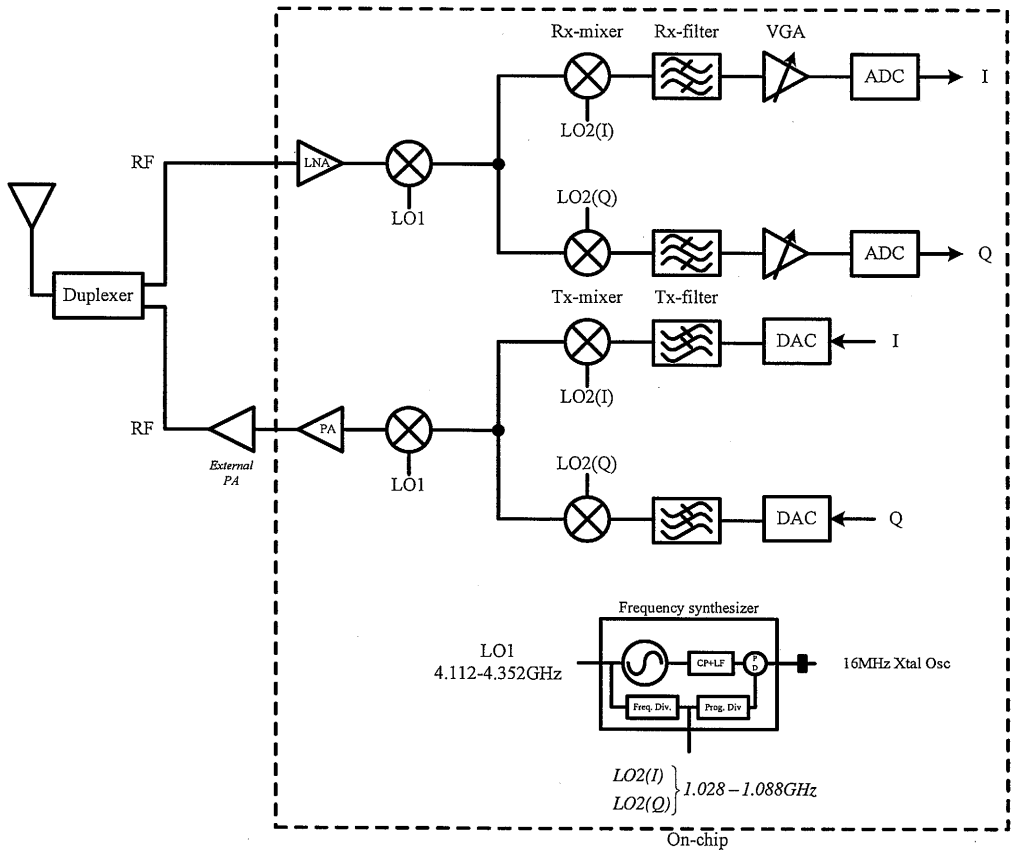


Fig. 3.6 Block diagram of the proposed zero-IF dual-conversion transceiver

3.4 Specification of the transceiver

3.4.1 Frequency planning of the proposed transceiver

For the transceiver's architecture shown in Fig. 3.6, the synthesizer needs to generate two LO outputs with the second LO (LO2) having both in-phase and quadrature-phase outputs. LO2 can be conveniently generated from LO1 using a frequency divider with a division ratio of n, i.e. $f_{LO1} = n \times f_{LO2}$. As such,

$$\begin{aligned} & f_{rf} - f_{lo1} - f_{lo2} = 0 \Rightarrow f_{rf} - f_{lo1} - \frac{f_{lo1}}{n} = 0 \\ & \Rightarrow f_{lo1} = \left(\frac{n}{n+1}\right) f_{rf} \end{aligned} \tag{3.1}$$

For n = 2, the second LO would be too high to be appropriate for low-power applications. For n = 3 or 5 or any other odd values, the required frequency dividers would be much more complicated than even-modulus counterparts. In particular, the

speed of these odd-modulus frequency dividers would be limited due to much larger parasitics.

As an optimal choice, n = 4 is used for the proposed frequency synthesizer because only 2 divide-by-2 dividers are required, which are much simpler to be implemented than dividers with odd modulus at very high frequency. Moreover, the second divider can drive larger loading due to the lower input frequency. Theoretically, n can be any multiple of 4. Yet, higher multiples of 4 are not desirable in terms of image rejection of the receiver. The image frequency can be represented by the following equation,

$$f_{im} = 2f_{lo1} - f_{rf} = f_{rf}\left(\frac{n-1}{n+1}\right) \tag{3.2}$$

When n increases, the RF signal gets much closer to the image signal. This deteriorates the image rejection particularly when the image signal falls within the passband of the LNA and mixer. The mechanism of image rejection, when n=4, has already been shown in Fig. 3.5. Under such a scenario, the image at 3GHz can be easily attenuated by the limited bandwidth of LNA and mixer.

For the lower and middle band of IEEE 802.11a transceiver, the specified f_{rf} ranges from 5.15GHz to 5.35GHz. Therefore, the resultant LOs are,

$$\begin{cases} LO1 = 4.144 - 4.256GHz \\ LO2 = 1.036 - 1.064GHz \end{cases} \tag{3.3}$$

3.4.2 System specifications for the receiver

3.4.2.1 Conversion gain

The output of a VGA should usually be resistive. In this design, an impedance around 300Ω is assumed to be connected at its output. The optimum single-ended

voltage swing for an ADC operating under 1-V supply is assumed to be $0.25V_p$. This implies that the differential output power for the VGA is,

$$10\log\left(\frac{0.5^2}{2(300)}\frac{1}{1m}\right)dBm \approx -4dBm \tag{3.4}$$

After the output level of the receiver is specified, the gain of the receiver can be calculated. The maximum gain of the receiver is required when the input power to the receiver is minimum, which is -82dBm for a data rate of 6Mb/s. In order to maintain the same output power, the required maximum gain for the receiver is,

$$-4dBm-(-82dBm)\approx 78dB \tag{3.5}$$

When the input power applied to the receiver is the minimum required in the standard, which is -30dBm for a data rate of 54Mb/s, the gain of the receiver is adjusted to be minimum. The required minimum gain for the receiver is,

$$-4dBm-(-30dBm)\approx 26dB \tag{3.6}$$

As a result, the gain of the receiver has to be adjusted from 26dB to 78dB to generate the same output power level with different input power levels.

Since the input and output impedance of the receiver are different, the above power gain is equivalent to a voltage gain of 34dB to 86dB in order to deliver the same differential output voltage level of -9dBV.

3.4.2.2 Bit error rate (BER)

In order to derive the noise figure required by the receiver, the packet error rate (PER) specified in the standard is used. The receiver is required to have a packet error rate less than 10% at a PSDU length of 1000 bytes, which is equivalent to 8000 bits, for all the modulation and data rates.

It is important to rewrite the aforementioned specification in terms of bit error rate because it helps to find the E_b/N_0, SNR and, hence, the noise figure required in the receiver. The probability of a packet received without error is $(1\text{-}BER)^{8000}$. This implies that the specification for the PER can be written mathematically as,

$$1-(1-BER)^{8000} < 0.1 \tag{3.7}$$

Therefore, the bit error rate, *BER*, should be less than 1.32×10^{-5}.

3.4.2.3 Signal-to-noise ratio

After the BER is determined, E_b/N_0 and *SNR* can be obtained. Fig. 3.7 shows the curves of *BER* against E_b/N_0 for different modulation and coding rates. The modulation 64-QAM with coding rate 3/4 calls for the largest E_b/N_0, given the same *BER*. With a *BER* of 10^{-5}, E_b/N_0 is equal to 12dB. After taking into account for around 20% margin, this is the minimum value of E_b/N_0 required to attain the specified *PER*.

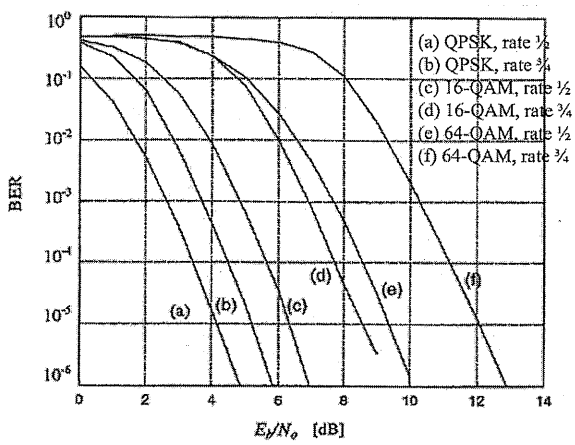


Fig. 3.7 BER VS Eb/N0 in AWGN for a constraint length 7 convolutional code

Signal-to-noise ratio can be written as,

$$SNR = \frac{P_{in}}{N_{in}} = \frac{P_{in}}{BW \cdot N_0} \tag{3.8}$$

where P_{in} is the input signal power, N_{in} is the input noise, BW is the occupied bandwidth and N_0 is the spectral noise density

It is closely related to E_b/N_0, which can be written as,

$$\begin{aligned}\frac{E_b}{N_0} &= \frac{P_{in}}{N_0} \cdot \frac{T_{sym}}{n_{sym}} \\ &= SNR \cdot BW \cdot \frac{T_{sym}}{n_{sym}}\end{aligned} \tag{3.9}$$

where T_{sym} is the OFDM symbol duration, n_{sym} is the number of bits for each ODFM symbol

It has already been shown that a E_b/N_0 of 12dB is required for the modulation 64-QAM with coding rate 3/4. In such modulation, the number of bits for each sub-carrier is 6 and the number of data sub-carrier is 48. Hence, the total number of bits for a symbol is 288. In IEEE 802.11a, the ODFM symbol duration is 4μs and the occupied bandwidth is 16.6MHz. The signal-to-noise ratio can be calculated as follows,

$$\begin{aligned}SNR &= \frac{E_b}{N_0} \cdot \frac{n_{sym}}{T_{sym}} \cdot \frac{1}{BW} \\ &= \frac{E_b}{N_0} \cdot \frac{288}{4\mu} \cdot \frac{1}{16.6M} = \frac{E_b}{N_0} + 6.4dB\end{aligned} \tag{3.10}$$

Therefore, a SNR of *18.4dB* is required for the receiver.

3.4.2.4 Noise figure

Noise figure of a receiver can be derived by the following equation,

$$\begin{aligned}NF &= P_{in} - N_{in} - SNR_{out} \\ &= P_{in} - N_0 - 10\log BW - SNR_{out} \\ &= P_{in} + 174dBm/Hz - 10\log BW - SNR_{out}\end{aligned} \tag{3.11}$$

For the modulation 64-QAM with coding rate 3/4, the minimum input power level is -65dBm and the SNR, obtained in the last section, is 18.4dB. As a result, the noise figure required for the receiver is

$$NF = -65 - 18.4 + 174 dBm/Hz - 10\log 16.6M = 18.4 dB \qquad (3.12)$$

By allowing for the attenuation of the antenna filter and leaving more margins for different building blocks, the targeted noise figure of the receiver is 10dB.

3.4.2.5 Out-of-channel third order input intercept point

The intermodulation product generated by the interferers located at the adjacent channels, as shown in Fig. 3.8, reduces the signal-to-noise ratio of the spectrum in the desired channel.

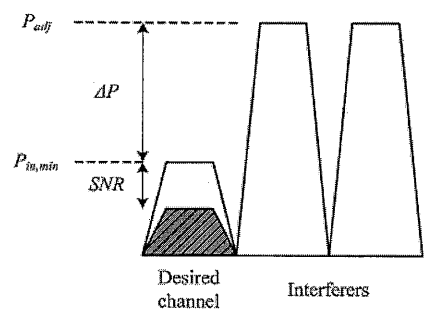


Fig. 3.8 Intermodulation products generated by the interferers adjacent to the desired channel

Because the specified *SNR* can only be attained when the intermodulation product is below the desired channel, the following equation can be written,

$$IIP3_{\min} = P_{in,\min} + \frac{P_{adj} - P_{in,\min} + SNR}{2} \qquad (3.13)$$

The worst scenario is the case when the modulation is 64-QAM with coding rate 3/4. In using such modulation, the minimum input power is -65dBm. The maximum output power of the transmitter is 16dBm. From the Friis free space equation, path loss is defined as,

$$Path\ loss = 20log\left(\frac{4\pi d}{\lambda}\right) \tag{3.14}$$

where d is the transmission distance and λ is the wavelength of the transmitting signal

It is assumed that the transmitter is 10cm away from the receiver in the worst-case scenario. By subtracting the path loss from the maximum output power of transmitter, the maximum interferer at the input of receiver is,

$$\begin{aligned} P_{adj} &= 16 - 20log\left(\frac{4\pi(0.1)}{3\times10^8 / 5.25\times10^9}\right) \\ &= -10.8dBm \end{aligned} \tag{3.15}$$

As mentioned in the previous section, the SNR required is 18.4dB. Thus, the minimum IIP3 required is,

$$IIP3_{\min} = -65 + \frac{-10.8-(-65)+18.4}{2} = -28.7dBm \tag{3.16}$$

In order to allow for some margin, the target value of the minimum IIP3 is -20dBm.

3.4.2.6 Peak-to-average ratio and 1-dB compression point

Peak-to-average ratio is the ratio of the instantaneous peak value of the time-averaged value of a signal. In OFDM systems, the peak-to-average ratio (PAPR) plays a significant role in determining the linearity performance of the systems.

In an OFDM system, the theoretical value of PAPR when all the sub-carriers are in phase is [14],

$$PAPR = 10\log N \tag{3.17}$$

where N is the number of sub-carriers

In IEEE 802.11a, the number of sub-carriers, including both the pilot and the data sub-carriers, is 52. The theoretical value is then 17.2dB. Yet, this theoretical value is overestimated in a practical case because if the data sub-carriers are well-scrambled, they rarely reach their peak, especially when the constellation size is large. An upper bound for PAPR is derived in [15]. It is shown that for a large number of sub-carriers, the PAPR of almost all OFDM symbols is bound by $2\ln N$. The resultant upper bound for PAPR is 9.0dB.

Techniques for peak reduction based on amplitude clipping or some forms of coding in the baseband processor [16] can be further used to reduce the PAPR to a value below 9dB. For the sake of simplicity, a PAPR of 9.0dB is used in this design.

1-dB compression point of the receiver is related to the maximum input power and the PAPR. It can be expressed as,

$$P_{1dB} = P_{in,\max} - PAPR \tag{3.18}$$

In the standard, the maximum input power to the receiver at the antenna is -30dBm. By assuming a 3dB drop by the antenna, the maximum input power to the LNA of the receiver is -33dBm. This implies that the 1-dB compression point should be larger than -33+9dBm=-24dBm.

3.4.2.7 I/ Q imbalance

The I/Q imbalance requirement for different modulation is shown in Table 3.1 [17]. The modulation, 64-QAM with data rate at 54Mbps, requires the smallest values of gain and phase imbalance.

Data rate /Mbps	Modulation scheme	Constellation error /dB	Gain imbalance	Phase imbalance
12	QPSK	-10	1.9	25.62

18	QPSK	-13	1.36	18.14
24	16-QAM	-16	0.97	12.84
36	16-QAM	-19	0.69	9.09
48	64-QAM	-22	0.49	6.43
54	64-QAM	-25	0.34	4.56

Table 3.1 I/Q imbalance requirements for various modulation schemes in IEEE 802.11a

By using signal processing techniques as mentioned in [18], distortion due to IQ imbalance can be estimated and compensated in the baseband processor in digital domain. In the compensation schemes, algorithms including post Fast Fourier transform (FFT) least square and least mean squares (LMS) equalization is utilized. After applying such schemes, the IQ imbalance in analog domain can be relaxed. Yet, in order to allow for margins for the IQ imbalance requirements, a gain imbalance of 0.4dB and phase imbalance of 5° is set as the target.

3.4.3 System specifications of the transmitter

3.4.3.1 Conversion gain

The output loading of the digital-to-analog converter, DAC, is resistive. In this design, the full-scale current of the DAC is 1.5mA with 1-V supply. This implies that the single-ended output voltage of DAC is 0.15Vpp with 100Ω loading. The differential input power to the transmitter is, thus,

$$10\times\log\left(\frac{1}{2}\cdot\frac{(0.3)^2}{2(100)}\cdot\frac{1}{1m}\right)=-3.5dBm \qquad (3.19)$$

In IEEE 802.11a, the required output power of the transmitter for the lower band is 16dBm. The total power gain of the transmitter is then 19.5dB.

Because the input and output impedance is different, the voltage gain of the transmitter differs from its power gain. The output voltage derived from the output

power is 2.0Vp. In decibel unit, this is equivalent to an output voltage of 3dBV. The voltage gain of the transmitter is *3-(-19.5)=22.5dB*.

However, an output voltage of $4.0V_{pp}$ is too large for a CMOS power amplifier. Thus, the target output voltage of the on-chip power amplifier is set to $0.6V_{pp}$, which is equivalent to -13dBV or 0dBm. An external power amplifier is used to boost the gain of the transmitter with a 16dBm output.

3.4.3.2 Spectrum mask

Spectrum mask is expressed in dBr, which is a measure of the spectral density relative to the maximum value in dB. It is the limits of spectral density at different frequency offsets The output spectrum of the transmitter should fall within the spectrum mask specified. The detail of the spectrum mask in IEEE 802.11a is specified in Table 3.2.

Frequency offset /MHz	Transmitted spectral density /dBr
9	0
11	-20
20	-28
30	-40

Table 3.2 Spectrum mask specified with limits on the transmitted spectral density at different frequency offsets.

An example of the OFDM output spectrum of the transmitter, generated by simulation in Matlab, is shown in Fig. 3.9. It is obvious that the simulated output spectrum falls within the spectrum mask.

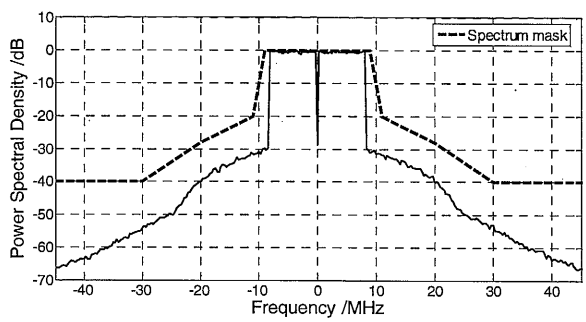


Fig. 3.9 Example OFDM output spectrum of the transmitter and its spectrum mask

It is interesting to note that the bandwidth of the OFDM signal in Fig. 3.9 expands outside the desired 20MHz bandwidth. It is better illustrated in Fig. 3.10 in which the "distorted" OFDM is compared with an ideal OFDM spectrum.

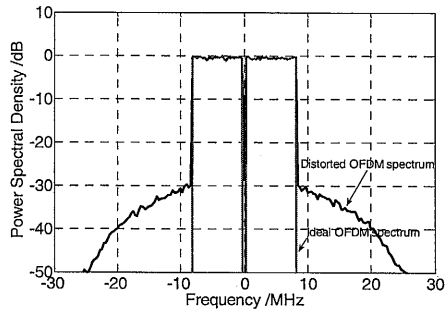


Fig. 3.10 Distorted and ideal OFDM spectrum

This phenomenon is called "spectral regrowth". Digital modulation schemes, like QPSK and QAM, are susceptible to spectral regrowth, in which a modulated spectrum is not limited to the desired bandwidth. It is caused by non-linearity in a system. To understand this phenomenon, an OFDM signal can be modeled as many discrete sub-carriers next to each other. All these discrete tones sub-carriers with each other and "regrow" outside the desired bandwidth.

For the sake of simplicity, only the two adjacent tones shown in Fig. 3.11 are considered. These two adjacent tones inter-modulate with each other and generate IM3 and IM5. Mixing reduces the power level of the intermodulation products. Higher order intermodulation products still exist but only IM3 dominates in most of the situations.

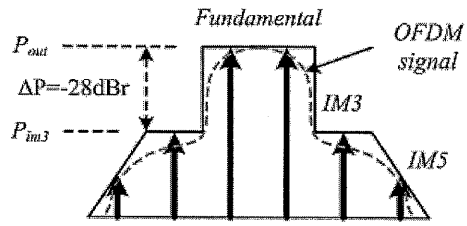


Fig. 3.11 An OFDM signal modeled as two adjacent tones

If only two adjacent tones are considered, the output-referred IP3 of the system should be written as,

$$OIP3_{\min} = P_{out} + \frac{\Delta P}{2} \tag{3.20}$$

Since the target output power of the on-chip power amplifier is 0dBm, the minimum required OIP3 of the transmitter is 14dBm.

3.4.3.3 LO leakage

Double conversion is achieved by the up-conversion mixer. The combination of the LO leakage of each up-conversion generates a center frequency component in the transmitter signal. Leakage of such component shall not exceed -15dB relative to the overall transmitter power, as specified in the standard.

3.4.3.4 Error vector magnitude (EVM)

Calculation of EVM involves the impairments in the analog part of the transmitter and the modulation scheme in the digital baseband processor. In order to derive the specification for non-linearity and power back-off performance for the transmitter, CAD tools like Matlab and ADS are used. Fig. 3.12 shows the constellation diagram of a transmitter when it achieves a value of EVM of 5.3%.

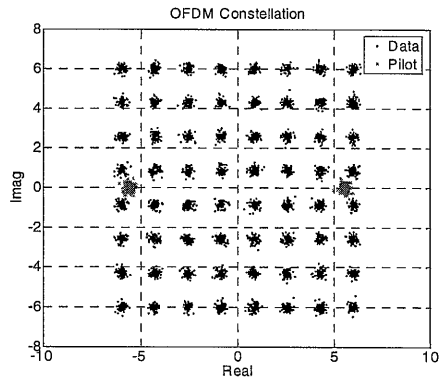


Fig. 3.12 Constellation diagram when EVM is 5.3%

In order to investigate the relationship of EVM with intermodulation parameters such as IIP3 and P_{1dB}, another CAD tool, *ADS*, is used for behavioral simulation of the transmitter with OFDM signals. The schematic of the transmitter is shown in Fig. 3.13.

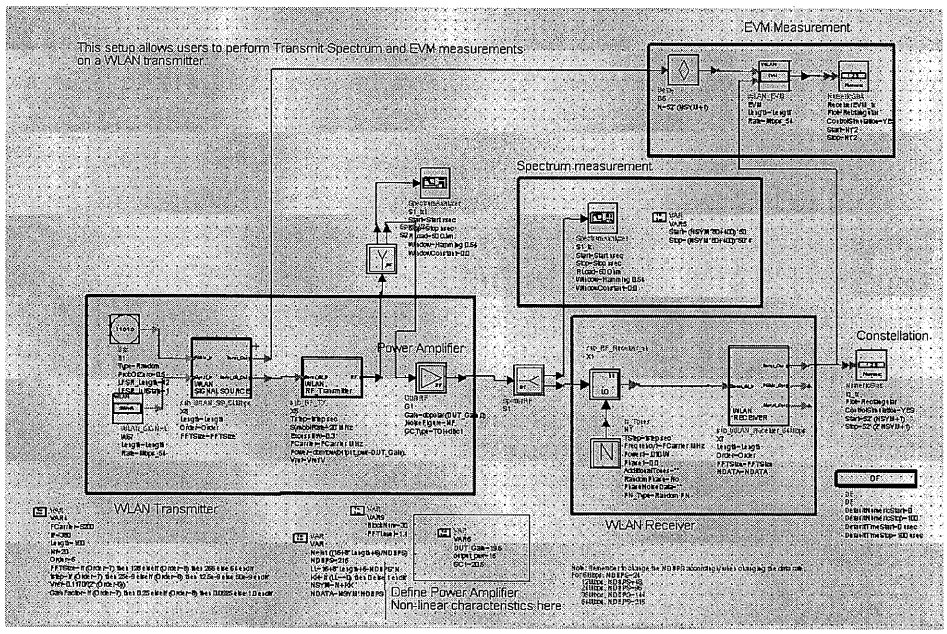


Fig. 3.13 Schematic for EVM measurement

The whole transmitter is modeled by a WLAN source, a quadrature modulator and a power amplifier. The power gain of the transmitter is set to be 19.5dB, which is the specified conversion gain derived in Section 3.4.3.1. The input and output power is -3.5dBm and 16dBm respectively. Non-linearity of the transmitter is modeled by

the power amplifier. The minimum 1dB compression point of the transmitter to achieve an EVM of 5.6% is found by sweeping the 1dB compression point of the PA. The simulation result is shown in Fig. 3.14. The minimum output-referred P_{1dB} required is 20.5dBm. An EVM as low as 1.5% is obtained when P_{1dB} is increased to 25dBm.

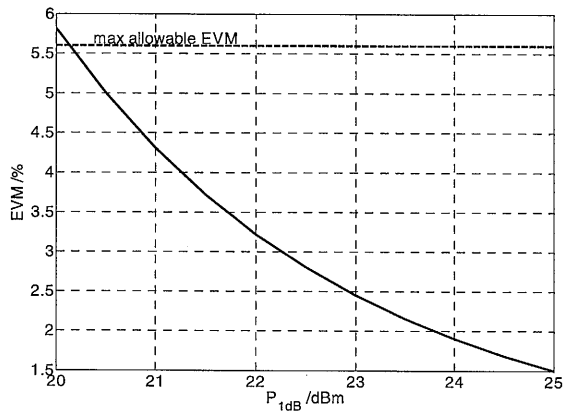


Fig. 3.14 EVM versus 1-dB compression point of the transmitter with external PA

P_{1dB} is then fixed and the output power of the transmitter is then swept from 6 to 16dBm. As shown in Fig. 3.15, a 10dB power back-off from the minimum P_{1dB}, 20.5dBm, reduces the EVM of the transmitter to a value of 1.2%.

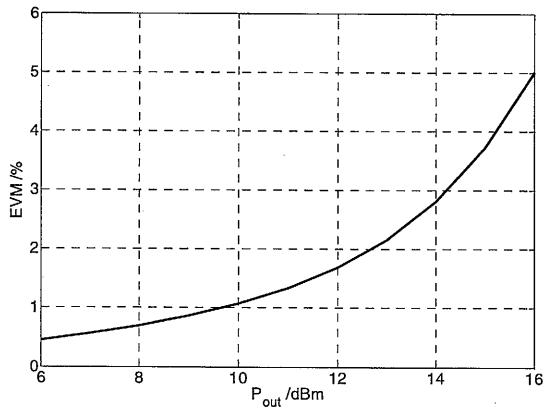


Fig. 3.15 EVM versus output power of the transmitter with external PA

As mentioned in Section 3.4.3.1, the target output power of the transmitter is 0dBm instead of 16dBm. Similar simulation is done using this value of output power. The power gain of the transmitter is adjusted to 3.5dB, with the same input power of -3.5dBm. Fig. 3.16 shows the EVM of the transmitter with the on-chip PA only against its P_{1dB}. The minimum output-referred P_{1dB} required is set to be 4.5dBm or -8.5dBV with an EVM of 5%. Since P_{1dB} and IP3 typically have a difference of 10dB, this corresponds to an output-referred IP3 of 14.5dBm. This is very close to the value derived in Section 3.4.3.2, which is 14dBm.

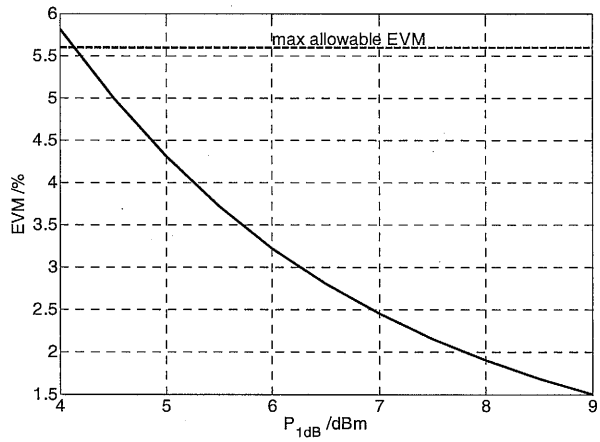


Fig. 3.16 EVM versus 1dB compression point of the transmitter without external PA

3.4.3.5 Phase noise requirement

It is assumed that for IEEE 802.11a the adjacent interferer is 40dB stronger than the desired channel. The worst-case SNR is 18.4dB, which corresponds to a BER of 10^{-5} in a 64-QAM system, as derived in Section 3.4.2.3. The phase noise required at the output of the frequency synthesizer is, therefore,

$$L\{20MHz\} = -40 - 10\log(20M) - 18.4 = -131.6 dBc/Hz \qquad (3.21)$$

By assuming a $1/f^2$ phase noise spectrum, the above phase noise corresponds to -105.6dBc/Hz@1MHz.

3.4.3.6 Spurious emissions

It is specified in the IEEE 802.11a standard that the spurs within and beyond 1GHz offset must be below -57dBm and -47dBm respectively.

All the specifications for the IEEE 802.11a transceiver are summarized in Table 3.3.

System	
Standard	IEEE 802.11a
Process	CMOS 0.18μm
Supply voltage	1V
Frequency Band	5.15-5.35GHz
No. of Channels	8
Channel bandwidth	20MHz
Modulation	BPSK, QPSK, QAM with OFDM
Highest data rate	54Mb/s
Rx	
Sensitivity	-82dBm (for 6Mb/s) -65dBm (for 54Mb/s)
Max. input signal	-30dBm
Conversion voltage gain	34-86dB
PER	<10%
BER	$<10^{-5}$
SNR	>=18.4dB (for 64-QAM)
Noise figure	< 10dB
Out-of-channel IIP3	>=-20dBm
Input-referred P_{1dB}	>=-24dBm
IQ imbalance	0.4dB (gain), 5° (phase)
Tx	
Output power	16dBm (w/ ext PA) 0dBm (w/o ext PA)
Input power	-3.5dBm
Conversion voltage gain	22.5dB (w/ ext PA) 9.5dB (w/o ext PA)
EVM	<=5.6% or -25dB
Out-of-channel IIP3	>=14dBm (w/o ext PA)
Input-referred P_{1dB}	>=4.5dBm (w/o ext PA)
Frequency synthesizer	
Spurious emissions <1GHz	<=-57dBm
Spurious emissions >1GHz	<=-47dBm
Phase Noise of LO	<=-131.7dBc@20MHz

Table 3.3 Summary of specifications for IEEE 802.11a transceiver

Chapter 4 Frequency Synthesizer

4.1 Existing solutions

The main drawbacks with the synthesizer in [19] include a high supply voltage of 2.5V and large power consumption of 180mW, which accounts for more than 70% of the total power of the whole receiver. It also requires an off-chip LPF, which is not suitable for monolithic applications. The frequency synthesizer reported in [20] generates two LO signals at 1/3 and 2/3 of the RF frequency, respectively. All components are integrated on-chip, but the supply voltage is 2.5V, and the power consumption is as high as 93mW.

Recently, a low-voltage frequency synthesizer that can operate at a supply voltage of 1V with a power consumption of 27mW was reported [21]. Phase-switching programmable divider is used to help reduce the power consumption. Techniques are also introduced to allow operation using a low-voltage supply. As an example, frequency-tuning mechanism in the VCO is done by varying the transconductance of the coupling transistors, and the current-driven-bulk technique is employed to reduce the threshold voltage of the PMOS transistors. It demonstrates that reducing the supply voltage can be one efficient way to shrink the power consumption. Yet, it is interesting to note that half of the power in the whole synthesizer is still dissipated by the VCO alone.

This chapter presents the design of a monolithic integer-N CMOS frequency synthesizer for WLAN IEEE 802.11a consuming only 9.7mW at 1-V supply. The proposed synthesizer employs a novel ultra-low-voltage VCO using transformer feedback and a stacked frequency divider. The synthesizer's specification and

proposed architecture are addressed in Section II. Detailed analysis and circuit implementation of the proposed VCO and of the first-stage frequency divider are presented in Section III. Section IV describes the design of other building blocks including remaining dividers, charge pump, phase-frequency detector (PFD), and loop filter. Section V presents all the measurement results of the proposed synthesizer together with detailed comparison with other state-of-the-art synthesizers.

4.2 Circuit specification of the frequency synthesizer

The synthesizer is designed to meet all the specifications mentioned in Chapter 3 with a supply voltage of 1V and a maximum power consumption of 10mW. The targeted chip area, including all passive components, should be less than $2mm^2$ using CMOS 0.18μm process. The specifications for the frequency synthesizer are summarized in Table 4.1.

Process	CMOS 0.18μm
Supply voltage /V	1
Power consumption /mW	<10
Tuning range (LO1) /GHz	4.144-4.256
Tuning range (LO2) /GHz	1.036-1.064
Reference frequency /MHz	16
No. of channels	8
Division ratio	259-266
Phase Noise of LO /dBc/Hz	<-131.6@20MHz
Spurious emissions <1GHz offset /dBm	<=-57
Spurious emissions >1GHz offset /dBm	<=-47

Table 4.1 Summary of specifications of the frequency synthesizer

4.3 Proposed synthesizer architecture

Two most popular architectures of frequency synthesizers are *integer-N* and *fractional-N*. Settling time and channel bandwidth, which is inversely proportional to the input reference frequency, are two of the most critical factors that determine the architecture to be used. In this design, the channel bandwidth is 20MHz, which is not variable and relatively large. It poses no limitation on the settling time requirement of the design. Thus, a simple integer-N architecture is selected rather than its much more complicated fractional-N counterpart.

The architecture of the frequency synthesizer is chosen to be a type-2, fourth-order loop using a charge pump as shown in Fig. 4.1. Compared to a lower-order loop, the additional poles provide higher spurious filtering and thus reduce the spurs generated by the input reference without decreasing the loop bandwidth or increasing the settling time and the chip area.

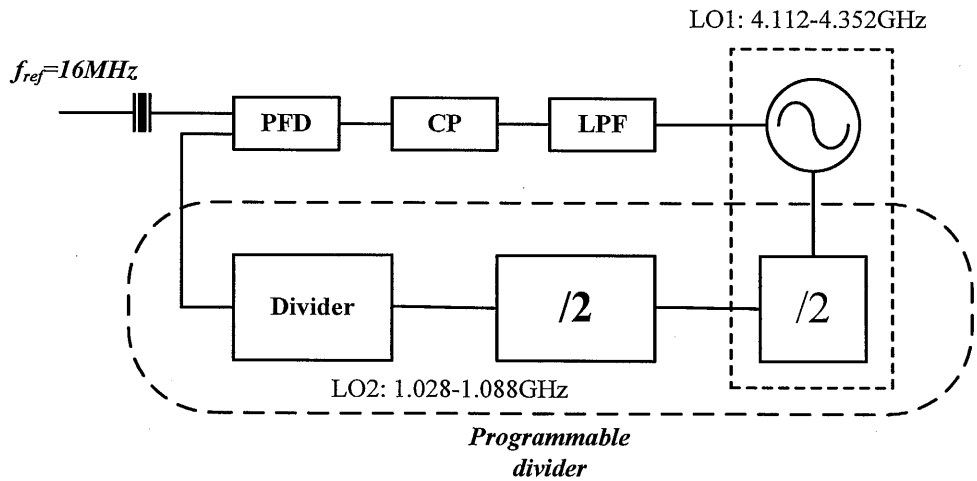


Fig. 4.1 Architecture of the proposed frequency synthesizer

In IEEE 802.11a, the total number of channels for the lower and middle bands is 8. This corresponds to a minimum range of division ratio of 259-266 from the output of the VCO to the reference input.

For 20MHz channel bandwidth, the reference frequency required in the proposed frequency synthesizer is *20MHz×(4/(4+1))=16MHz*. As a rule of thumb, the loop bandwidth is chosen to be less than one tenth of the reference frequency for the sake of stability. In this case, a loop bandwidth of around 80kHz is selected and the phase margin is chosen to be around 50° to ensure stability and to minimize the settling time.

In order to determine other parameters of the frequency synthesizer, the linearized PLL model shown in Fig. 4.2 is considered. Using this model, the transfer function of the closed loop can be represented by the following equation,

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{NK_pK_{vco}Z(s)}{Ns + K_pK_{vco}Z(s)} \tag{4.1}$$

where N is the total division ratio, K_p is the charge pump gain, K_{vco} is the VCO gain and $Z(s)$ is the transfer function of the loop filter

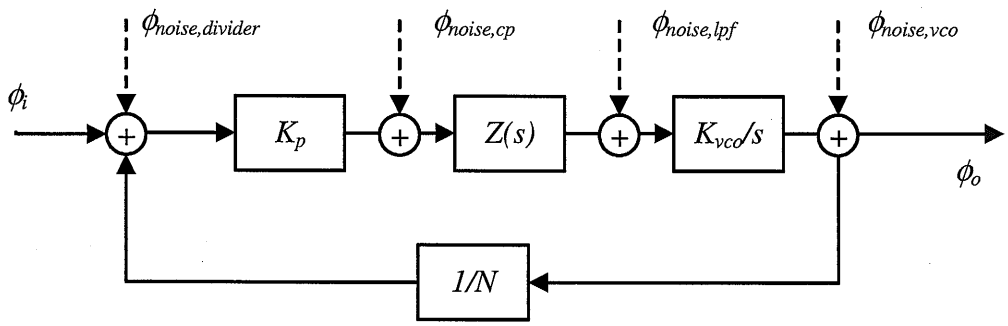


Fig. 4.2 Linearized PLL model of the frequency synthesizer

The loop filter to be used is third-order, as shown in Fig. 4.3, whose transfer function can be represented by the following equations.

$$Z(s)=\frac{R_1C_1s+1}{sC_1\left(1+\frac{C_2}{C_1}+\frac{C_3}{C_1}\right)\left[A(R_1C_1s)^2+B(R_1C_1s)+1\right]}$$

$$where\begin{cases}A=\dfrac{\dfrac{C_1}{C_2+C_3}}{\dfrac{C_1}{C_2+C_3}+1}\dfrac{R_3C_3}{R_1C_1}\dfrac{C_2}{C_1}\\[2ex] B=\dfrac{1+\dfrac{C_1}{C_2+C_3}\dfrac{R_3C_3}{R_1C_1}\left(1+\dfrac{C_2}{C_1}\right)}{1+\dfrac{C_1}{C_2+C_3}}\end{cases} \tag{4.2}$$

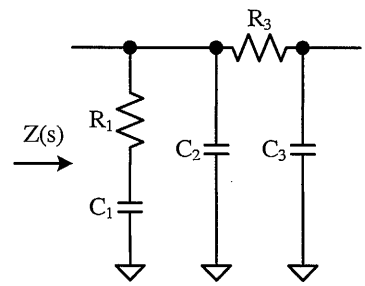


Fig. 4.3 A third-order loop filter

In order to ensure that the phase noise specification is also fulfilled, the same phase model shown in Fig. 4.2 is used again. In the figure, phase noise contributed by each building block is represented by the dashed arrow. The contribution from each building block is calculated individually and finally summed at the output node, by superposition, in the phase model to obtain the total phase noise.

By optimizing the other loop parameters, the open-loop frequency response of the frequency synthesizer as shown in Fig. 4.4 is obtained. The simulated loop bandwidth and phase margin is 79kHz and 53° respectively. The corresponding phase noise contribution of each building block and the total phase noise are shown in Fig. 4.5.

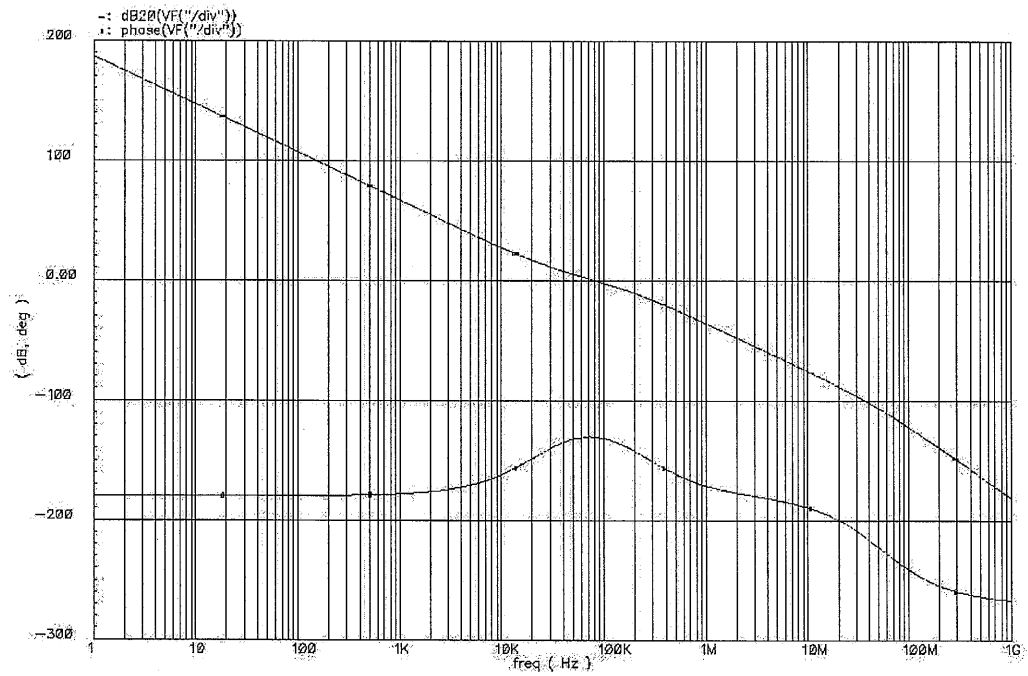


Fig. 4.4 Simulated loop bandwidth and phase margin

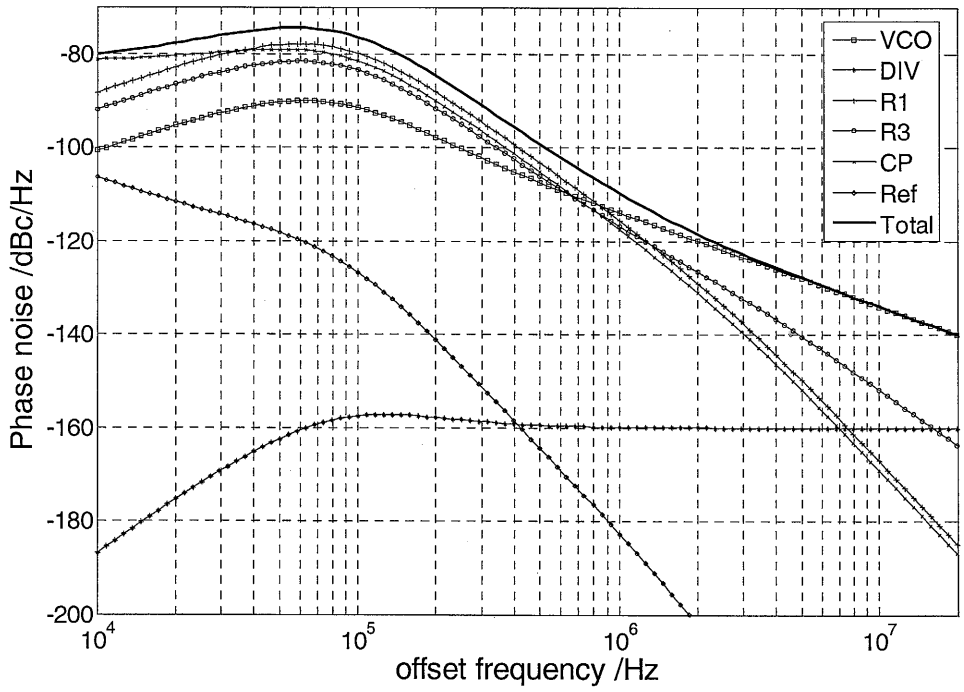
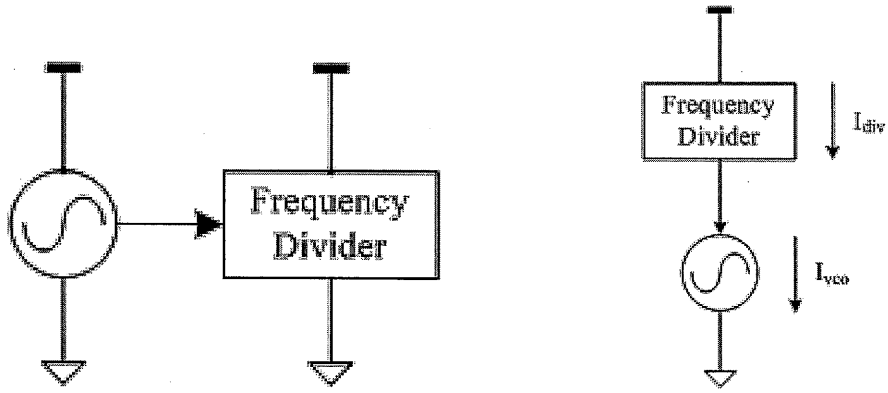


Fig. 4.5 Simulated phase noise of each building block and the whole system

4.4 Circuit implementation

4.4.1 VCO design

Conventionally, the VCO and the first divider-by-2 in a frequency synthesizer are biased by two independent currents from the same supply voltage as shown in Fig. 4.6. Assuming that, at the same current level, the VCO can operate under supply voltage smaller than the divider, or vice versa, power cannot be fully utilized in such design. To save power, a low-voltage divider is proposed to be stacked on top of a low-voltage VCO. The current flowing out of the divider is reused by the VCO, and the power can be reduced as long as the supply voltage can be the same.



Existing solution Proposed solution

Fig. 4.6 Existing and proposed solution

The proposed VCO is based on the conventional Colpitts oscillator for low phase noise. It has been explained in [22] that the Colpitts oscillator has superior phase noise performance as a result of the cyclo-stationary noise properties. In order to enhance the performance of the Colpitts VCO at a low supply voltage, the capacitor divider is replaced by a transformer. The transformer-feedback topology proposed in [23] as shown in Fig. 4.7 was considered to realize the required VCO below 1-V supply. For this topology, the signal at the drain can swing above supply, and the signal at the source can swing below ground. This mechanism results in an

increase of the effective supply voltage. The other feature of the VCO is the positive feedback given by the transformer, which helps to increase the total signal swing. Alternatively, for given operation frequency and output swing, the transistor sizes and the total power consumption can be reduced when compared to the conventional design.

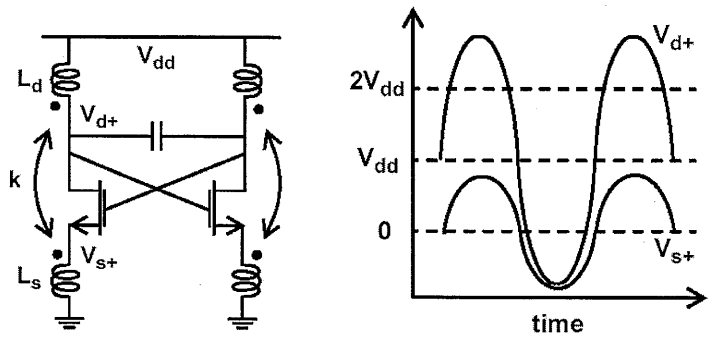


Fig. 4.7 Low-voltage VCO using transformer-feedback technique [23]

There are at least two possible ways of stacking the frequency divider onto a VCO. However, the VCO in [23] is not suitable for use with a stacked frequency divider because the divider would be connected in series with the transformer, as shown in Fig. 4.8. Such series connection degrades the quality factor of the drain inductor by the impedance looking into the bottom of the divider. Instead, a common-drain configuration is employed, in which transformer feedback between the gate and the source of the transistor is used in the proposed VCO. Similar to the aforementioned VCO [23], this type of transformer feedback also increases the signal swings at both the gate and the source and thus increases the effective voltage supply. The signal swing is also increased by the positive feedback of the transformer. Moreover, by removing the capacitor divider, the equivalent capacitance at the VCO output can be reduced, which help increase both the quality factor Q and the output voltage of the resonant tank.

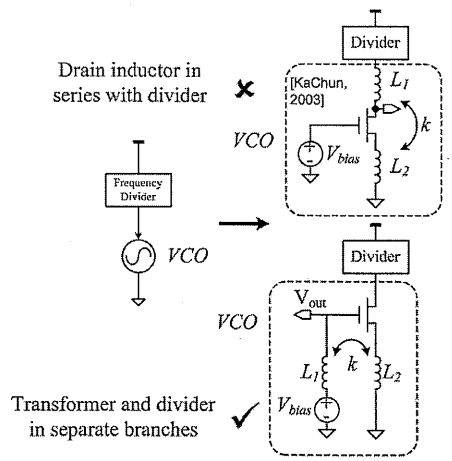


Fig. 4.8 Evolution of the proposed low-voltage VCO

The stacking of the divider directly onto the VCO also enhances its performance since such topology facilitates the connection of the two building blocks using a very short metal wire in the layout. This is critical to the performance of the whole frequency synthesizer because the non-negligible transmission-line effect of every connection may pose serious problems at such high frequency.

The following equation can then be derived from Fig. 4.9,

$$\frac{v_x}{i_x} = \frac{g_m\omega^2\left(M^2 - L_1M\right) + s\left(L_1 - g_m{}^2\omega^2\left(M^2 - L_1L_2\right)\left(L_2 - M\right)\right)}{1 + g_m{}^2\omega^2\left(L_2 - M\right)^2} \tag{4.3}$$

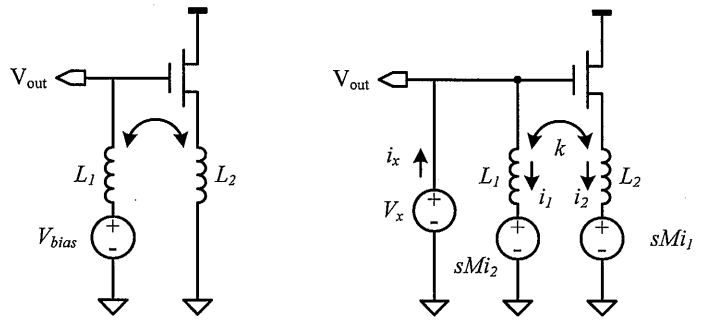


Fig. 4.9 Schematic and equivalent circuit of the proposed oscillator using transformer-feedback

Similar to the Colpitts oscillator, for the best performance, the ratio of L_1 and L_2 is determined to be around 4. The mutual inductance is then always smaller than the

primary inductance for $L_1 > L_2$ and $M > 0$. The term $\left(M^2 - L_1 M\right)$ is always negative for M>0 and, therefore, the real part of the above equation provides a negative resistance to compensate for the loss of the inductor and the capacitor. The imaginary part of the above equation resonates with the parasitic capacitance and the varactor and determines the resonant frequency.

The source of the oscillating transistor is connected to the secondary coil instead of ground. Since it has been shown previously that the source can swing below ground, it is necessary to put the transistor in a deep N-well to ensure that its bulk is shorted together with the source and that the substrate-source junction is not forward biased. The zero substrate-source voltage helps to reduce the threshold voltage of the oscillating transistor as well. In addition, the deep N-well can provide better isolation to the substrate noise.

As shown in Fig. 4.10, a very small negative gm cell using NMOS is connected at the VCO output to enhance the quality factor of the primary coil. Similarly, a very small negative gm cell using PMOS is connected at the secondary coil to enhance its quality factor. Noise contribution from these small negative gm cells is negligible. The differential signal swing at the outputs of the VCO is equivalent to the gate-drain voltage across the transistors in the negative gm cell. Because the differential signal swing is larger than the threshold voltage, the transistors in the negative gm cell go into the linear region, at a particular point of every oscillation cycle. If the common node of the NMOS negative gm cell is connected to ground directly, the momentarily small transconductance given by those transistors in the linear region reduces the average impedance of the resonant tank. Current sources, always working in the saturation region, are used to bias both of the negative gm cells to prevent this problem [24]. Since the impedance looking into these current sources is large they

can help to remedy this problem by preventing the negative gm cells from reducing the quality factor of the resonant tank.

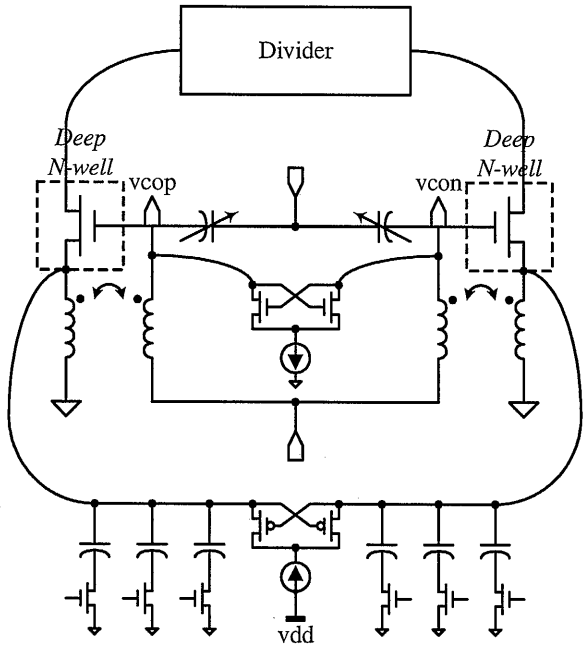


Fig. 4.10 Other features of the VCO

Switched capacitor array is being added to the VCO in order to compensate for the process variations. However, by adding SCA at the output of the VCO, extra parasitic capacitance will be added. This will not only reduce the resonant frequency but also lower the tank voltage. An approach to minimize the effect of the parasitic capacitance is to connect the SCA to the secondary coil instead of the primary coil. Because the ratio of the primary to secondary inductance is smaller than one, the sensitivity of the parasitic capacitance at the secondary coil to the oscillation frequency is much smaller than that at the primary coil. Hence, the resonant frequency and tank voltage are not significantly affected.

The same approach can be applied to the varactor, which is implemented as an accumulation-mode varactor in the design. However, assuming the same size of varactor, the effective frequency tuning range due to the varactor alone will be

reduced by connecting it to the secondary coil instead of the primary coil because of the reduced sensitivity as mentioned before. This is not favorable for application in the IEEE 802.11a standard because of the relatively wide channel bandwidth and low-supply voltage operation, which would set a limit on the effective minimum tuning range of the varactor.

The phase noise of the VCO is calculated using the linear, time-varying (LTV) model proposed by [22], which can be represented by the following equation,

$$L\{f\} = \frac{1}{8\pi^2 f^2 q_{\max}^2} \sum_n \left(\frac{\overline{i_n^2}}{\Delta f} \Gamma_{rms,n}^2 \right) \tag{4.4}$$

The impulse sensitivity function (ISF), the noise-modulating function (NMF), and their product, referred to as the effective ISF [22], are obtained by direct simulation in SpectreRF. Perturbation, in the form of current impulses injected at different phases of the oscillation waveform, causes different phase shift in the waveform. By sweeping the time of the current injection, the impulse response of the phase shift at the VCO output can be obtained. The resultant ISF, NMF and the effective ISF are shown in Fig. 4.11. The calculated RMS value of the effective ISF is 0.3, which is smaller than the typical value of conventional LC oscillator (~0.5). The phase noise of the VCO is also simulated using directly the periodic steady state (PSS) analysis in SpectreRF under identical conditions. The phase noise plots using the above two methods are shown and compared in Fig. 4.12. They are very close together with the maximum deviation located at the largest frequency offset, which is 20MHz as shown in the figure. The calculated phase noise using the LTV model and the simulated phase noise using PSS in SpectreRF are -139.1dBc/Hz and -138.7dBc/Hz at 20MHz offset respectively. It can be concluded that the difference of the above two methods is within 0.5dB for all the frequency offsets.

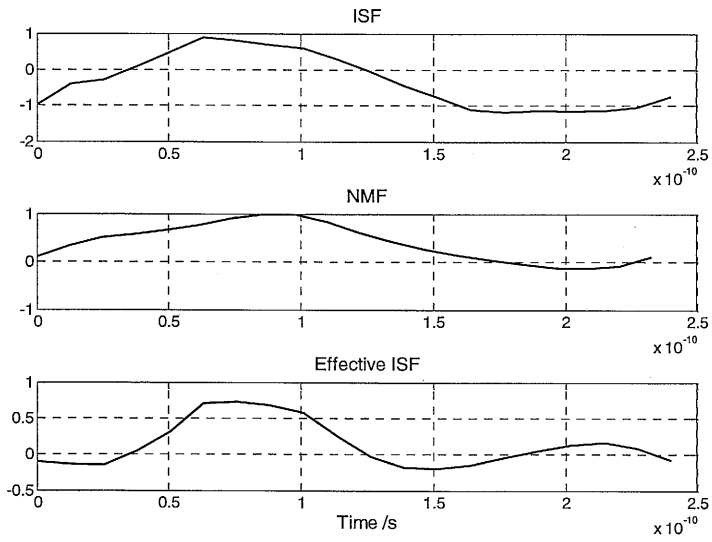


Fig. 4.11 ISF, NMF and effective ISF of the VCO

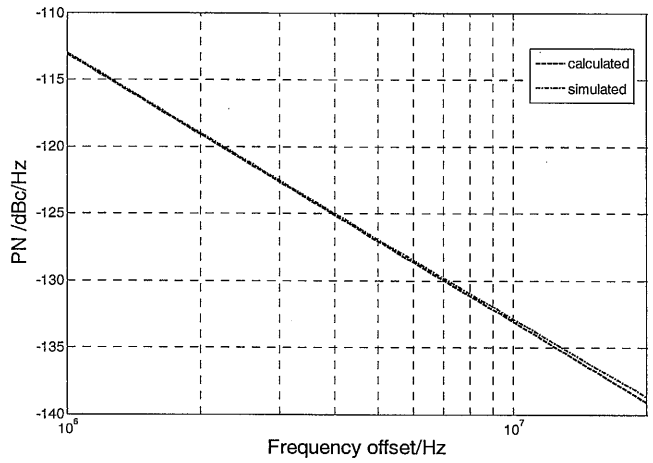


Fig. 4.12 Simulated and calculated phase noise of VCO

4.4.2 First divide-by-2 frequency divider

AC current from the VCO is then injected directly into the frequency divider. Because a common-drain configuration is used, the frequency divider can be stacked in series at the drain without degrading the performance of the VCO. An injection locked divider (ILD) is one of the potential candidates. It is especially useful for low-voltage supply because of the inductive load. However, the locking range of the ILD alone is limited. Small deviation in the load inductance may cause out-of-lock

and thus failure of the whole design. In order to have a higher frequency tuning range, variable capacitors can be connected at the output of the ILD and the VCO. However, frequency tuning would have to be done by adjusting the resonant frequency of the VCO and the ILD altogether. This would increase the complexity of the frequency synthesizer. In order to remove this complex mechanism, a source-coupled logic (SCL) frequency divider, which usually has much larger input locking range than its counterpart, is used to replace the ILD.

The SCL divider consists of 2 SCL, active-load, D-latches connected in a master-slave configuration. The tail current sources are removed, and the transistors for the complementary clocks are replaced by the same transistors used in the VCO. Since active-load SCL frequency divider usually has much wider input frequency tuning range, frequency tuning can then be achieved by the VCO alone. In addition, by using active load in the SCL divider, no inductors are needed, and the chip area can be minimized. Since the divider is in the master-slave configuration, quadrature signals are automatically available at the outputs of the divider.

The SCL divider may self-oscillate when no input signal is applied or when the ac current injected is too weak, which would be the case if the oscillation of the VCO is relatively weak. In the worst-case scenario, the self-oscillation of the divider would dominate and overcome the oscillation of the VCO. This would shift the desired frequency ranges and degrade the total phase noise performance. As a result, it is critical to design the divider carefully to make sure that it has a maximum locking range and it is not strong enough to dominate the oscillation.

The full schematic of the proposed design is shown in Fig. 4.13. The differential transient voltage outputs of the VCO and the divider as well as the ac differential

currents injected into the dividers are simulated using SpectreRF and shown in Fig. 4.14. The divide-by-two operation is clearly illustrated in the figure.

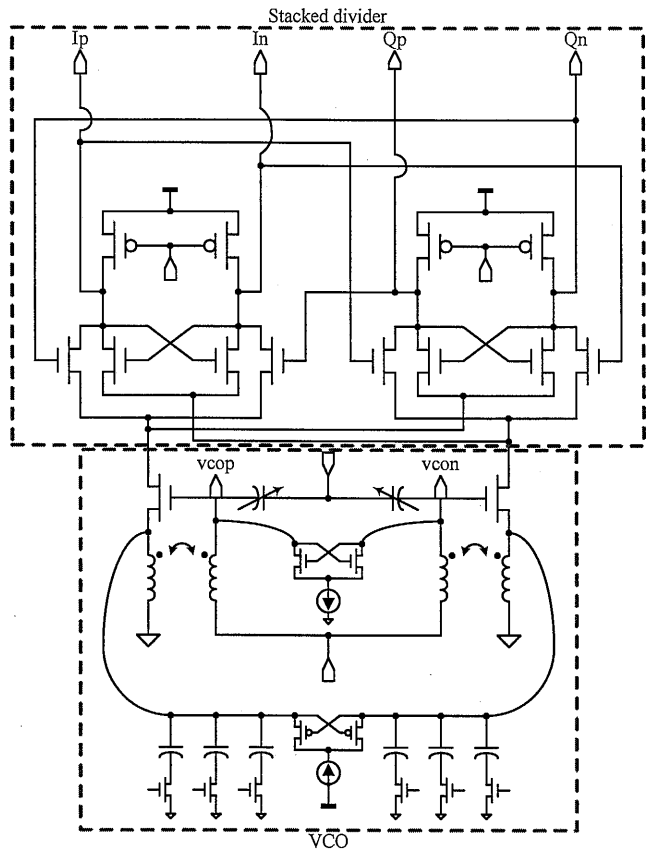


Fig. 4.13 Schematic of the proposed VCO and divider

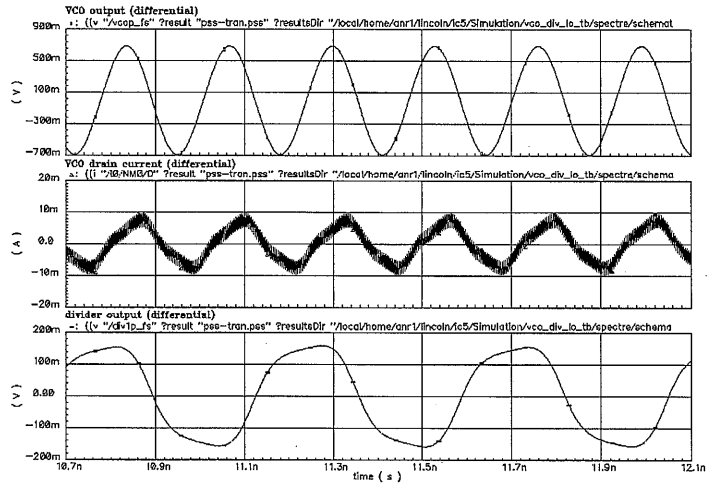


Fig. 4.14 Simulated voltage and current waveforms at the outputs of the VCO and dividers

4.4.3 Other Building Blocks

4.4.3.1 Programmable divider

The frequency allocations and their corresponding division ratio of the frequency divider are shown in Table 4.2. The division ratio specified ranges from 259 to 266, and it is achieved by using a phase-switching programmable divider [25]. The main reason is that its first divider can be implemented by a simple divide-by-2 frequency divider, as opposed to a dual-modulus prescaler as in the pulse-swallowing approach [26]. Only two flip-flops in a master-slave configuration are required to operate at the maximum frequency in the divide-by-2 frequency divider, in contrast to the many flip-flops used in the dual-modulus prescaler. Also, there is no need to handle high-frequency signals to reset the flip-flops in the divide-by-2 frequency divider. Due to its simplicity, divide-by-2 frequency divider can operate at much higher frequency than the dual-modulus prescaler. More complicated structures, such as the MUX, divide-by-N divider and state machines are still required. However, these building blocks no longer limit the input frequency of the programmable divider because their operating frequency is already divided down. Their power consumption can also be significantly reduced.

Channel No.	RF	LO1	LO2	Div. Ratio
36	5.18	4.144	1.036	259
40	5.2	4.16	1.04	260
44	5.22	4.176	1.044	261
48	5.24	4.192	1.048	262
52	5.26	4.208	1.052	263
56	5.28	4.224	1.056	264
60	5.3	4.24	1.06	265
64	5.32	4.256	1.064	266

Table 4.2 Frequency allocations and the corresponding division ratio

However, the conventional phase-switching approach suffers from glitches when the phase switching is done with improper signal timing from the phase control

block [27]. In order to remove the potential glitches, backward phase-switching technique [28] is used. Instead of advancing one cycle for every phase switching, one cycle is stepped back for every phase switching. Similar to the conventional forward [25] approach, the modulus of the programmable divider is changed by controlling the number of times of phase switching in one cycle. Moreover, instead of using two divide-by-2 stages in the conventional phase-switching approach, one more divide-by-2 stage is added, which will generate 8 phases for the phase-select stage, as shown in Fig. 4.15. This extra divide-by-2 operation further relaxes the frequency requirement of the phase select stage, which includes an 8-to-1 MUX, asynchronous dividers, a modulus control block, and an 8-bit shift register. This can help to reduce the power consumption as well.

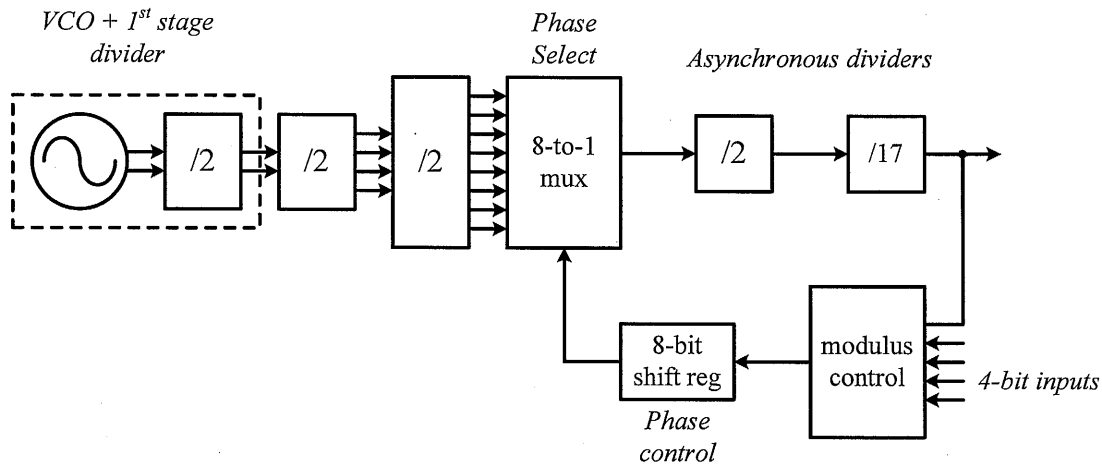


Fig. 4.15 Block diagram of the programmable divider using backward phase switching

The design and operation of the programmable divider is described and explained below. Because the minimum number of channels specified is 8, the number of input bits for the modulus control should be at least 4. This is equivalent to a maximum number of 15 phase switching. For backward phase switching, the

smallest modulus required, which is 259 in this case, rather than the largest one, is used to determine the division ratios of the asynchronous divider. Together with the first three divide-by-2 operations, a division ratio of 34 is eventually selected for the asynchronous divider to cover the smallest modulus specified. The operation of the programmable divider can be summarized by the following equation,

$N=2\times2\times2\times2\times17-s$ where s=number of phase switching from 0-15

Since the maximum number of phase switching is 15, the modulus of the programmable divider ranges from 257 to 272, covering the whole frequency tuning range in the specification.

4.4.3.2 Second-stage frequency divider

The first-stage frequency divider is already stacked onto the VCO, as mentioned before. The other critical divider is the second-stage divide-by-2, which operates at half of the maximum frequency. It is implemented by SCL frequency divider, as shown in Fig. 4.16. Similar to the first-stage frequency divider, it consists of 2 SCL, active-load, D-latches connected in a master-slave configuration. For operating at low-voltage supply, the tail current source is removed. Instead, AC coupling is used to bias the divider. The 2 D-latches are driven by a pair of complementary clocks. The four separate transistors in conventional design for the complementary clock inputs in the two D-latches are merged into two, *Mclka* and *Mclkb*. Quadrature signals are available at the outputs of the SCL divider. This helps to simplify the generation of second quadrature LO signals for the IQ path of a transceiver in a double-conversion topology.

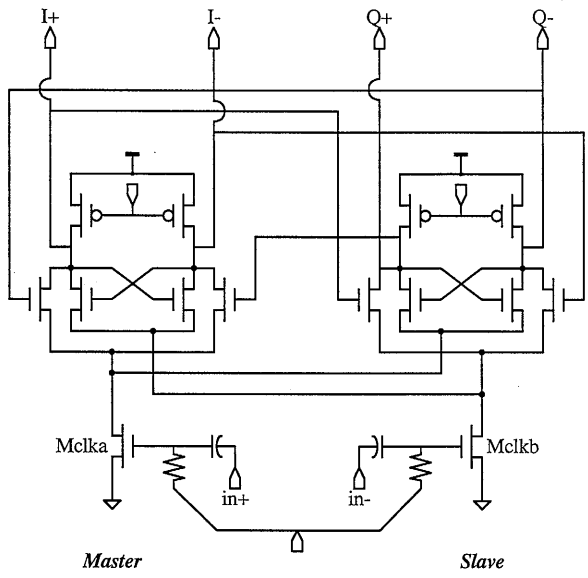


Fig. 4.16 Second-stage frequency divider

4.4.3.3 Third-stage divider

A divide-by-2 stage can generate 4-phase outputs. Thus, two divide-by-2 stages can be combined together to generate the 8 phases required for the phase-select stage. However, in such configuration, there may be 2 possible output states depending on the initial states of the latches. These possible states may cause errors in phase switching. A third-stage 8-phase divide-by-2 divider is implemented to tackle such problem.

The 8-phase divider consists of four D-latches cascaded in a ring, as shown in Fig. 4.17. Since the D-latches are connected in a ring, only one output state is possible. This avoids the aforementioned ambiguous states. The schematic of a D-latch is also shown in the same figure. NMOS is used for sensing and storing while PMOS is used for pull-up operation. Except the clock inputs, it has no stacked transistor and therefore enables low-voltage and high-speed operation. Once the input is low, the latch will store the input value. Full-swing outputs are available, which eliminates a need for using buffers between the divider and the latter CMOS

stages. Since the DC output of the second-stage divider is too high for the input PMOS transistor here, AC coupling is used to bias the divider.

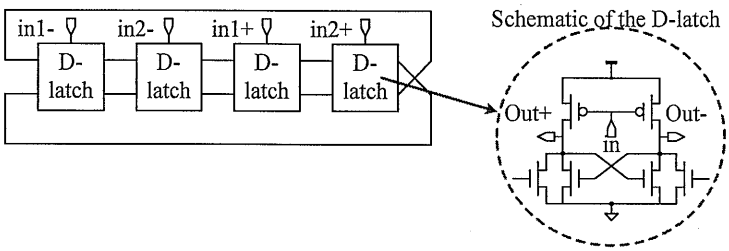


Fig. 4.17 Third-stage 8-phase frequency divider

4.4.3.4 Other stages in the programmable divider

The phase-select and phase-control stages are simply an 8-to-1 MUX and an 8-bit shift register respectively. The modulus control is also a MUX, in which the 4 inputs are used to control the 16 different moduli available in the divider. Because the speed requirement of these building blocks is not high, all of them are implemented using simple CMOS logic. For the asynchronous dividers, they are composed of a simple divide-by-2 stage in cascade with a divide-by-17 stage. TSPC logic is used to implement these two dividers. Fig. 4.18 shows the simulated input and output waveforms of the programmable divider, using SpectreRF, when the division ratio is set to its minimum, 259.

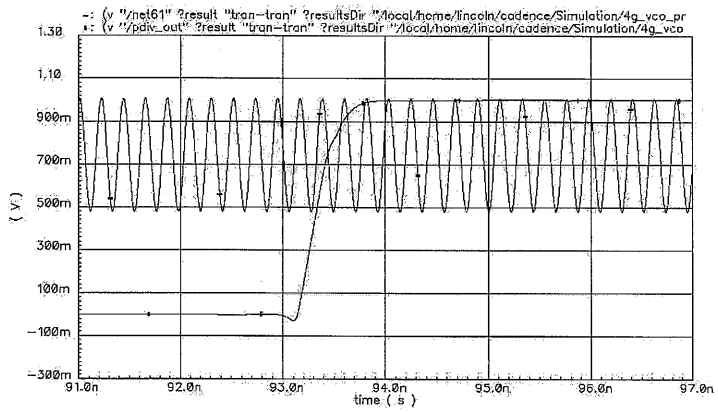


Fig. 4.18 Simulated input and output waveforms of the programmable divider

4.4.3.5 PFD, charge pump and loop filter

The connection of the PFD, single-to-differential converter, charge pump and loop filter is shown in Fig. 4.19. A typical PFD, as shown in

Fig. 4.20, is used. It is implemented in static CMOS logic. Buffers are added at the output of the NOR gate to increase the delay of the RESET signal to eliminate the problem of dead zone. A single-to-differential converter, as shown in Fig. 4.21, is used at the output of the PFD to provide complementary outputs for the charge pump.

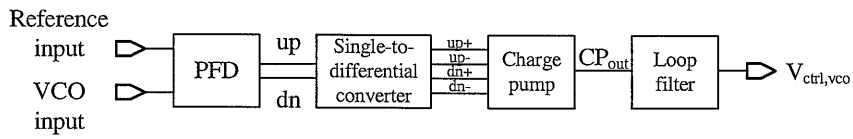


Fig. 4.19 Block diagram of the PFD, single-to-differential converter, charge pump and loop filter

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Fig. 4.20 Block diagram of the PFD

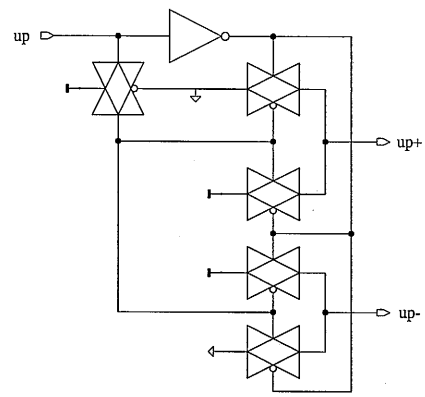


Fig. 4.21 Block diagram of the single-to-differential converter

The schematic of the charge pump is shown in Fig. 4.22. A unity-gain buffer is included to ensure that the voltages at nodes 1 and 2 are equal. This can help to

minimize the charge sharing effect between nodes 1, 3 and 4 and, thus, minimize the spurious tones at the VCO output.

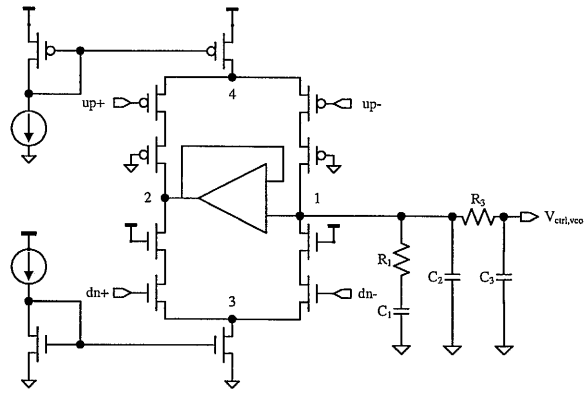


Fig. 4.22 Schematic of the CP and loop filter

A third-order passive loop filter is connected at the output of the charge pump. As mentioned previously, when compared to a second order passive loop filter, the additional pole helps to reduce the output spurs without reducing the loop bandwidth. The component values of the filter are summarized in Table 4.3. The total capacitance required in the loop filter is less than 100pF. The capacitors are implemented using MIM capacitors available in the process technology. This only occupies a total area of around 300×300μm^2, which is a reasonable value to be put on the chip.

Parameter	Value
Loop BW	79kHz
PM	53°
K_{vco}	200MHz/V
I_p	5μA
C_1	75.39pF
C_2	4.45pF
C_3	4.97pF
R_1	79.17kΩ
R_3	30kΩ

Table 4.3 Summary of filter parameters

4.4.3.6 Passive components

4.4.3.6.1 Transformer

The layout of the transformer used is shown in Fig. 4.23. It is realized with a 2-port Shibata coupler structure [29]. It consists of 2 spiral rectangular inductors using the top metal, interwinding with each other. Top metal is used because it is the most remote layer from the substrate, which helps to reduce the substrate loss, and it usually has the lowest sheet resistance. The primary coil has 2 turns while the secondary coil is made of 2 single turn inductors connected together in parallel. This can help to maximize the edge coupling between the two coils. The second topmost layer is used as the underpass to connect the coils to the output ports. The metal width of the coils is 20μm and the metal spacing is 3μm. The minimum spacing allowable in the process is used in order to increase the coupling between the coils. The outer dimension is 332μm×332μm while the dimension of the inner hole is 154μm×154μm.

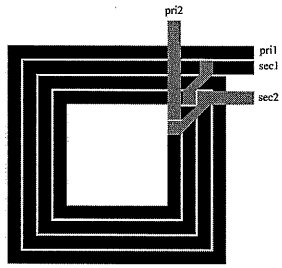


Fig. 4.23 Layout of the transformer

4.4.3.6.2 Accumulation mode MOS

It is formed by putting an NMOS inside an N-well, as shown in Fig. 4.24. When Vgs or Vgd is negative, electrons beneath the gate are pushed away and a depletion area is formed. The capacitance is the series connection of the oxide capacitance, Cox, and the depletion capacitance Cd. When the voltage is positive, electrons

beneath the gate accumulated. The total capacitance in this case is Cox. Hence, when the mode of operation is changed from depletion to accumulation, capacitance is changed from the minimum to the maximum values.

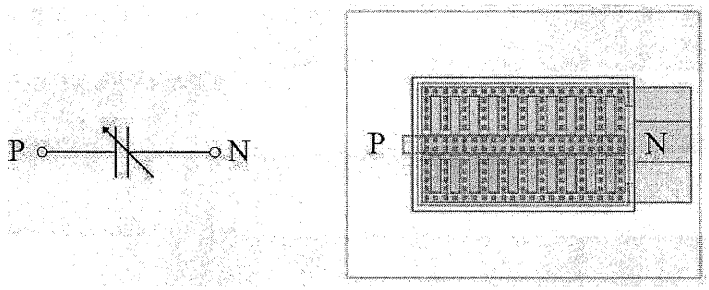


Fig. 4.24 Schematic and layout of the varactor

4.4.3.6.3 Metal-insulator-metal capacitor

MIMcap is formed by two parallel metal plates in square shapes. The top metal, metal 6, forms the upper electrode and the second top metal plate, metal 5, forms the lower electrode. The cross-section and top view of the layout is shown in Fig. 4.25. With the addition of a special layer, called capacitor-top-metal (CTM), the thickness of the dielectric layer between the two electrodes is reduced. This helps to increase the total capacitance. The effective capacitance per unit area of the MIMcap is around 1fF/μm^2.

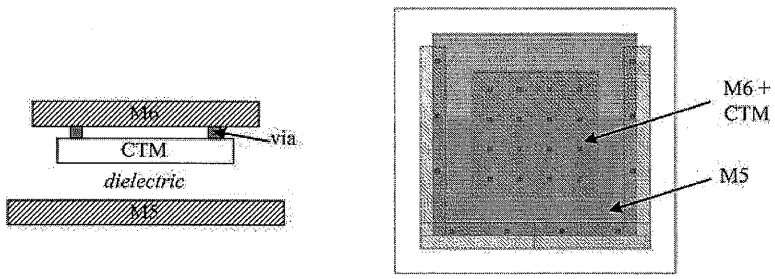


Fig. 4.25 Cross-section and top view of the layout of the MIMcap

4.4.3.6.4 Switching capacitance array

The schematic of an N-bit SCA is shown in Fig. 4.26. The parameters in the SCA are determined by the desired tuning range and qualify factor of the SCA.

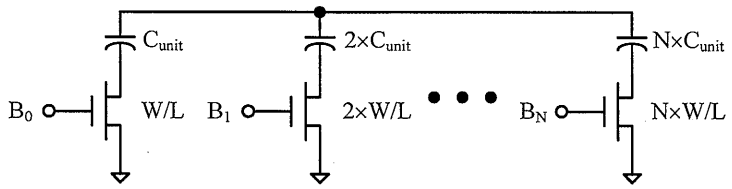


Fig. 4.26 Schematic of the SCA

The quality factor of each unit of the SCA can be written as,

$$Q = \frac{1}{\omega_0 C_{unit} R_{on}} \tag{4.5}$$

where R_{on} is the turn-on resistance of the switch in the triode region and

$$R_{on} = \frac{1}{\mu C_{ox}(V_{gs} - V_t)}\left(\frac{W}{L}\right)$$

The width of the MOS is proportional to the parasitic capacitance at its drain and inversely proportional to its turn-on resistance. Hence, increasing the width of the MOS reduces the tuning range of the SCA but increases its quality factor. This trade-off also explains why NMOS switches are used in the SCA because of its much larger mobility than PMOS.

The minimum capacitance of the N-bit SCA can be represented by the following equation,

$$\begin{aligned} C_{sca(\min)} &= C_{unit} \| C_d + 2 \times C_{unit} \| C_d + \cdots 2^{N-1} \times C_{unit} \| C_d \\ &= (2^N - 1)(C_{unit} \| C_d) \approx (2^N - 1) C_d \end{aligned} \tag{4.6}$$

where C_d is the parasitic capacitance at the drain of the MOS in the OFF state and $C_d << C_{unit}$

Similarly, the maximum capacitance of the SCA is,

$$\begin{aligned} C_{sca(\max)} &= C_{unit} + 2 \times C_{unit} + \cdots 2^{N-1} \times C_{unit} \\ &= (2^N - 1) C_{unit} \end{aligned} \tag{4.7}$$

In order to achieve continuous frequency tuning, capacitance tuning range of the the varactor has to fulfill the following equation,

$$C_{\mathrm{var}(\max)} - C_{\mathrm{var}(\min)} > C_{unit} - C_{unit} \| C_d \tag{4.8}$$

4.4.3.6.5 MOS capacitor

Although MiMcap is a linear capacitor, its small value of capacitance per unit area constitutes a pulling factor for small chip area. In order to reduce the chip area, NMOS capacitor in strong inversion is used as a second-choice capacitor in non-critical part of the circuit, which does not have a strict requirement for linear capacitance. Its layout and schematic is shown in Fig. 4.27. One of the terminals is formed by connecting the drain, source and body together and the other terminal is the gate. By connecting the gate terminal to a positive voltage much larger than the threshold voltage and the other terminal to ground, the MOS operates in strong inversion. The effective capacitance per unit area is around 8f/μm^2, which is 8 times larger than the MIMcap.

Since such type of capacitor is very non-linear and requires a large positive voltage, it is only used as a decoupling capacitor for all the analog and digital supplies in the circuit. It helps to minimize the interference and noise coupling into the supplies from the other parts of the circuit.

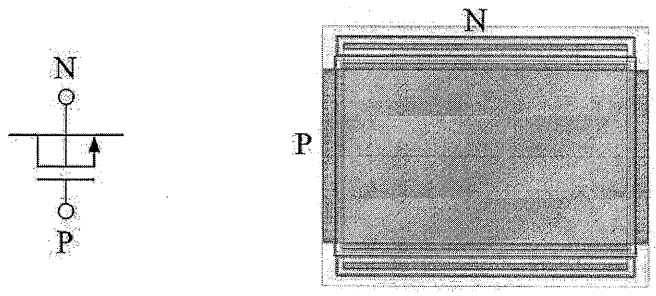


Fig. 4.27 Schematic and layout of the MOS capacitor

4.4.3.6.6 Guard rings

N-well and P-substrate taps are used as guard rings. N-well taps are connected to the supply pins and p-substrate taps are connected to the ground pins. They help to reduce substrate noise coupling. The layout of a device enclosed by double guard rings is shown in Fig. 4.27. P-substrate tap collects holes pass through the substrate and the N-well tap collects electrons. All the guard rings are broken to prevent the formation of loop current.

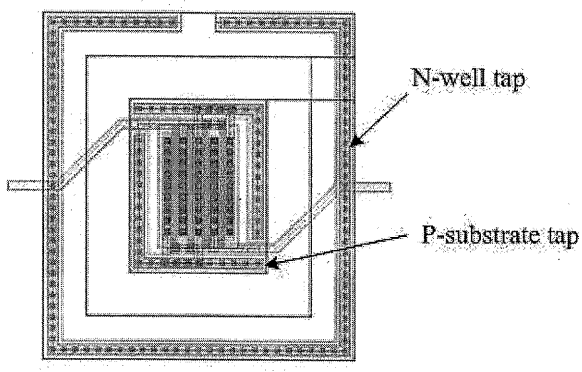


Fig. 4.28 A negative gm cell enclosed by double guard rings

4.5 Experimental results

The proposed frequency synthesizer is fabricated in 0.18□m CMOS process (VTn = 0.52 V, VTp = - 0.54 V) with 6 metal layers and MIM capacitor. Fig. 4.29 shows the die micrograph and floorplan of the proposed frequency synthesizer, which occupies a chip area of 1.28mm^2 only. No off-chip component is required.

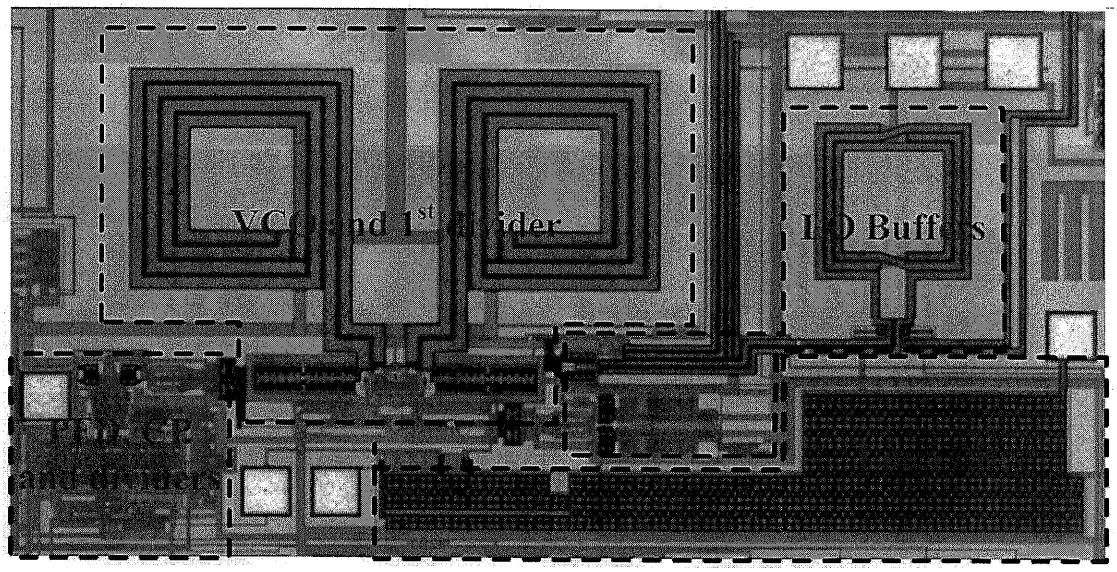


Fig. 4.29 Die micrograph of the frequency synthesizer

4.5.1 Testing setup for transformer

The network analyzer is used for characterization of the transformer. Before reading the measurement data from the device-under-test, the network analyzer has to be calibrated using the calibration substrates provided. Its purpose is to calibrate out the losses of the cables, microwave probes and the frequency dependence of the phase and amplitude characteristics in the cables and connectors. After the calibration, the reference plane is moved from the input/output connectors of the network analyzer to the microwave probe tips.

Separate testing structure for the transformer alone is included, as shown in Fig. 4.32. In the testing structure, two of the terminals in the four-port transformer are grounded. This configuration is the same as that in the VCO. In the VCO, one terminal of the primary coil is connected to a DC bias pin, which is equivalent to ac ground, and one terminal of the secondary coil is connected to ground directly. This configuration also allows for measurement using the two-port network analyzer. The setup for measuring the S-parameters for modeling is shown in Fig. 4.31.

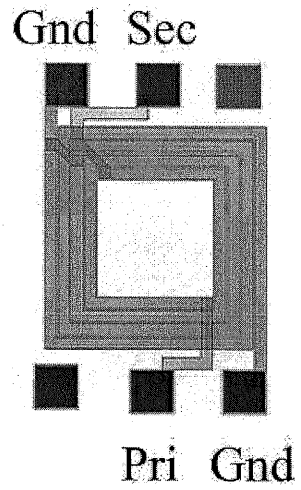


Fig. 4.30 Testing structure for the transformer

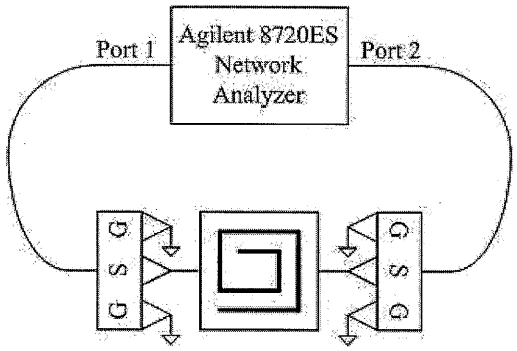


Fig. 4.31 Setup for measuring the S-parameters of the transformer

Pad de-embedding is very critical to the accuracy for the modeling of the transformer. Therefore, testing structures for calibration which consists of open and shorted pads are also included. Their respective S-parameters are also obtained by the use of the network analyzer, as show in Fig. 4.32 and Fig. 4.33.

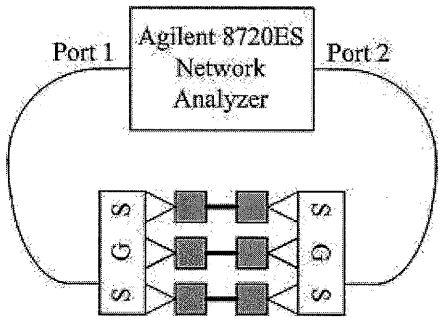


Fig. 4.32 Setup for calibrating the shorted on-chip pads

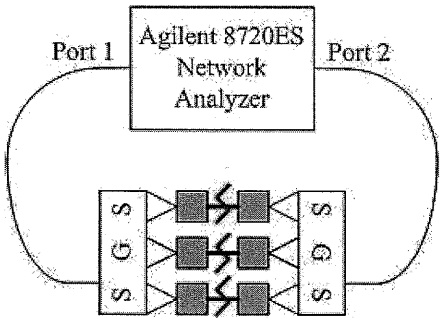


Fig. 4.33 Setup for calibrating the opened on-chip pads

After the measurement is done, the S-parameters, measured from the shorted pads and the transformer, are converted to Y-parameters. The Y-parameters of the shorted pads are subtracted from those of the transformer so as to cancel out the shunt parasitics due to the pads. Next, the resultant Y-parameters and the S-parameters of the open pads are converted to Z-parameters. The Z-parameters of the open pads are subtracted from those of the transformer. The purpose is to remove the series parasitics added by the pads. The calibration is complete after the subtracted Z-parameters are converted back to S-parameters. All these conversions and calculations are summarized and listed mathematically as follows,

$$\begin{cases} S_{xformer} \rightarrow Y_{xformer} \\ S_{open} \rightarrow Y_{open} \end{cases}$$

$$Y_{de1} = Y_{xformer} - Y_{open}$$

$$\begin{cases} Y_{de1} \rightarrow Z_{de1} \\ S_{shorted} \rightarrow Z_{shorted} \end{cases}$$

$$Z_{de2} = Z_{de1} - Z_{shorted}$$

$$Z_{de2} \rightarrow S_{cal}$$

4.5.2 Testing setup for the measurement of VCO

The setup for the measurement of the VCO alone is shown in Fig. 4.34. DC biases for the VCO are applied externally. The control voltage for the varactors, which are parts of the VCO, is fixed using off-chip bias for the testing of the VCO alone. The differential signals at the VCO outputs are input into the on-chip 50Ω open-drain buffer. The buffered signals are picked up by differential microwave probes, combined using a hybrid combiner and sent to the spectrum analyzer. Frequency, amplitude and phase noise are then measured using the spectrum analyzer. Current and power consumption is measured by multi-meters.

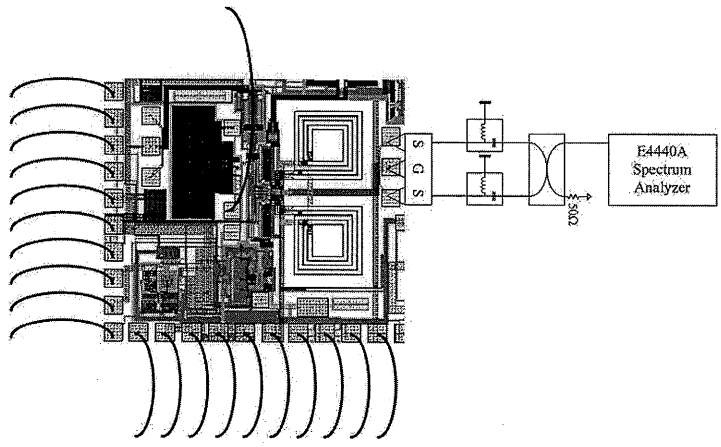


Fig. 4.34 Setup for the measurement of the VCO alone

Since there is power loss due to 50Ω open-drain buffer, coaxial cable and the probes, the signal obtained directly is not sufficiently large for accurate measurement of phase noise due to the inherent noise floor of the spectrum analyzer. External amplifier is used between microwave probes and the spectrum analyzer to amplify the signal before being injected into the spectrum analyzer.

By sweeping DC voltage applied to the varactor, the tuning curve for the VCO gain can be obtained.

4.5.2.1 Testing setup for the VCO and dividers

The setup for testing the VCO and the first and second dividers, shown in Fig. 4.34, is similar to that of the VCO except that the buffered signals at the output of the dividers are picked up by the probes instead.

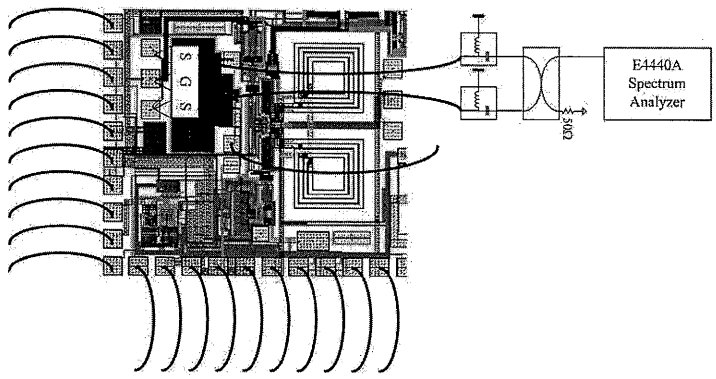


Fig. 4.35 Setup for the measurement of the VCO and the first and second dividers

After the above measurement is done, the VCO and the programmable divider together are tested. The setup is shown in Fig. 4.36. It is again similar to the previous setups except that the 16MHz output signal of the programmable divider is measured by a Hi-impedance probe, which is connected directly to an oscilloscope. All the division ratios are tested and verified using the oscilloscope.

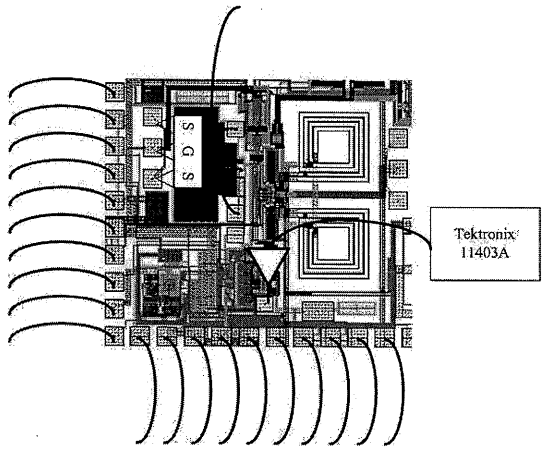


Fig. 4.36 Setup for the measurement of the VCO and all the dividers

4.5.2.2 Testing setup for the closed-loop frequency synthesizer

The setup is shown in Fig. 4.37. All the DC biases are applied externally. The reference frequency is injected into the frequency synthesizer using a clean signal generator. The output signals at the output of the first and second LOs are picked up by microwave differential probes. Functionality is verified by tryout all the division ratios of the frequency synthesizer. Again, due to the inherent noise floor of the spectrum analyzer, the signals are amplified by an external amplifier for the measurement of phase noise.

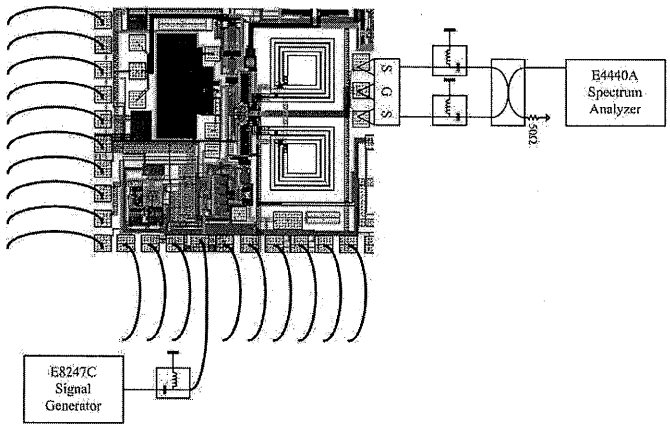


Fig. 4.37 Setup for the measurement of closed-loop frequency synthesizer

In order to test the settling time, square wave is applied to the programmable divider through the shift register to change the division ratio of the frequency synthesizer periodically. The control voltage used to adjust the varactor is also changed periodically to lock the VCO. By using an oscilloscope, one cycle of the rectangular wave representing the change in the control voltage can be observed and the settling time can be derived.

4.5.3 Measurement results of the frequency synthesizer

The S-parameters of the transformer are obtained by using the network analyzer. The wide-band model of the transformer, shown in Fig. 4.39, is used to fit

the measured S-parameters of the transformer. After fitting with S-parameters obtained in the 2-port measurement, the inductance of the primary coil is 1.66nH with a Q of 6.6 while the inductance of the secondary coil is 0.37nH with a Q of 6.5. The coupling between the 2 coils is measured to be 0.65. The resonant frequency of the transformer is much larger than 10GHz. This is good enough for the proposed frequency synthesizer.

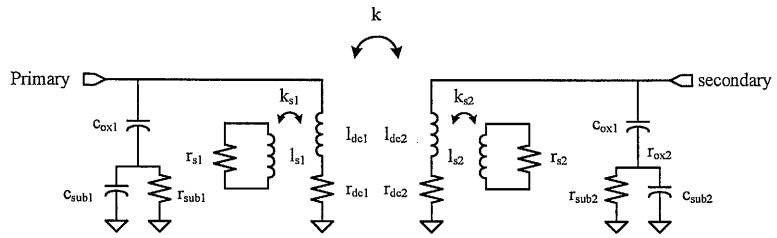


Fig. 4.38 A wide-band transformer fitting model

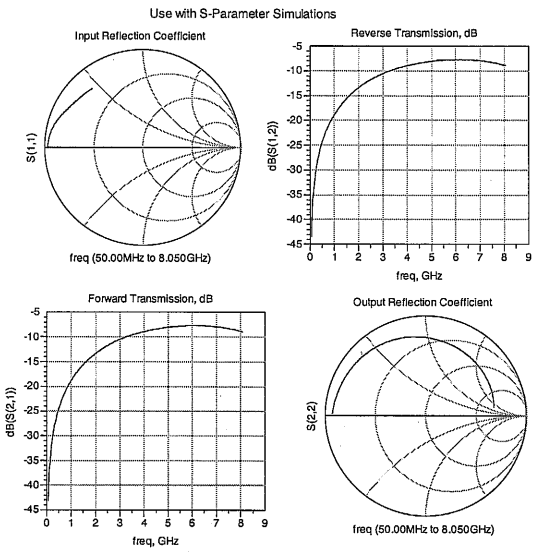


Fig. 4.39 S-parameters of the wideband model after model-fitting

The performance of the VCO was measured with the control voltage at the varactor being fixed externally. The output spectrum of the VCO is measured by Agilent E4440A, as shown in Fig. 4.40. The frequency tuning curve of the VCO, as shown in Fig. 4.41, is then obtained by varying the control voltage at the varactor

from 0V to 1.5V. Each curve represents the frequency variation corresponding to the control voltage at the varactor with different number of SCAs turned on. Only the linear part of the curve from 0V to 1V is used in the frequency synthesizer for the best performance under 1V supply. The VCO gain is measured to be around 200MHz/V in this linear region. By switching the SCA, together with the varactor, the VCO can be tuned from 3.58-4.5GHz. This corresponds to a tuning range of 920MHz (23%). Yet, the ultimate frequency tuning range in this frequency synthesizer is determined by the division ratio of the programmable divider, which is designed to start from 4.144GHz to 4.352GHz. This is close to a frequency range of 200MHz. Thus, a single combination of SCAs suffices for proper operation.

The phase noise of the VCO alone is measured, which is -140.5dBc/Hz at an offset of 20MHz with the carrier frequency being 4.36GHz, as shown in Fig. 4.42. The power consumption of the VCO together with the first-stage divider is 5.17mW. The figure of merits (FOM), including the power consumed by the first-stage divider, is 180.14. FOM is defined as,

$$FOM = 10\log\left[\left(\frac{\omega_0}{\Delta\omega}\right)\frac{1}{L(\Delta\omega)\times V_{DD}\times I_{DD}}\right] \tag{4.9}$$

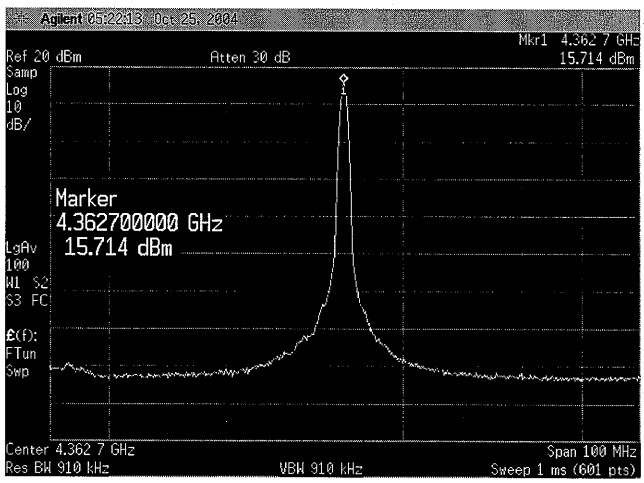


Fig. 4.40 Output frequency spectrum of the VCO in the unlocked state

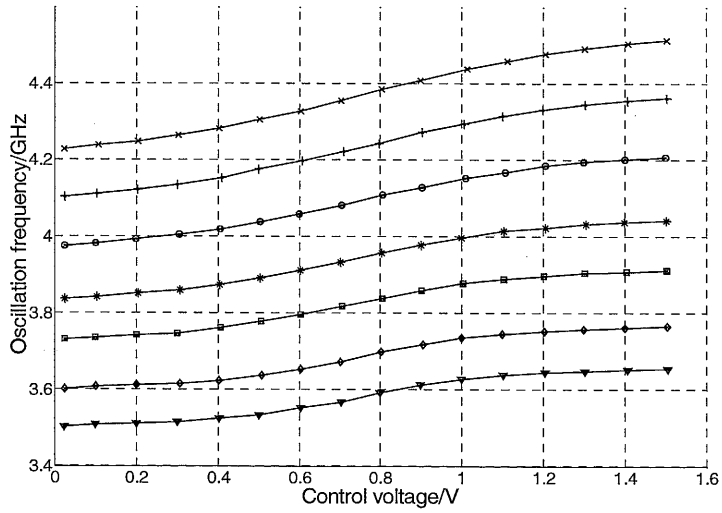


Fig. 4.41 Frequency tuning curves of the VCO by switching the SCAs

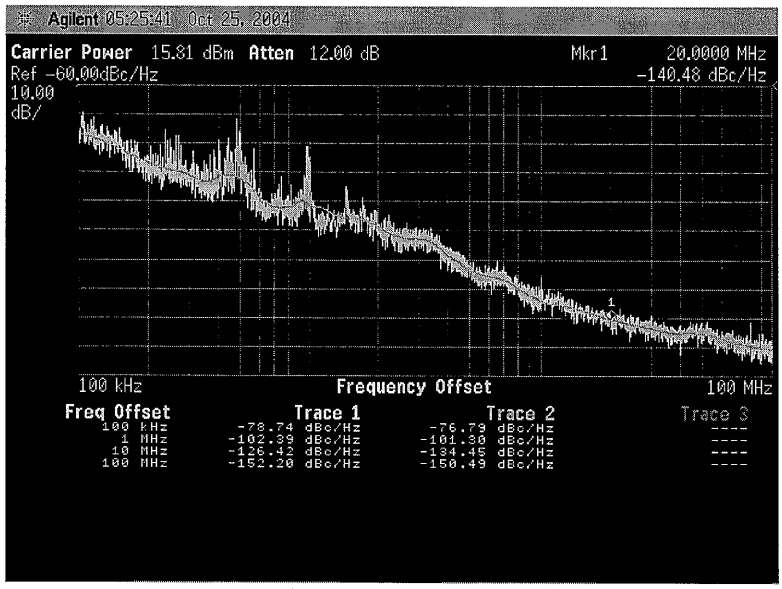


Fig. 4.42 Phase noise of the VCO in the unlocked state

The performance of the VCO and the dividers was then measured, also with the control voltage at the VCO being fixed externally. A high impedance probe is used to detect the signals at the output of the programmable divider. Its transient waveform, measured by Tektronix TDS 1012, is shown in Fig. 4.43. The output frequency of the divider is around 16MHz, which is close to the expected value.

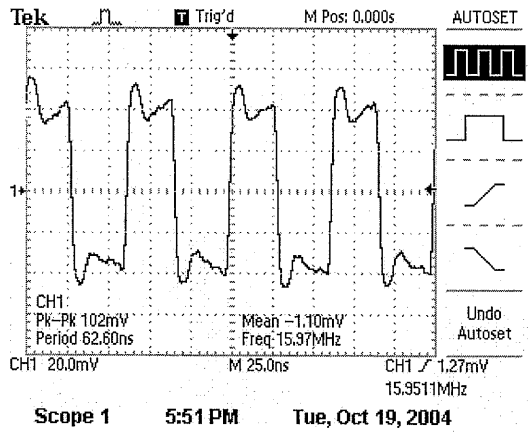


Fig. 4.43 Transient waveform at the output of the programmable divider

The loop was then closed with the connection of a 16MHz reference input generated by Agilent E8247C. The division ratio of the programmable divider is set to be 272, which is the largest value in this design. Fig. 4.44 shows the output frequency spectrum of the proposed frequency synthesizer. The spur is -75.5dBc at an offset of 16MHz from the carrier frequency of 4.352GHz. Its phase noise plot is measured by Agilent E4440A and shown in Fig. 4.45. The in-band phase noise at an offset of 10kHz is -71.1dBc/Hz and the out-of-band phase noise at an offset of 20MHz is -140.1dBc/Hz.

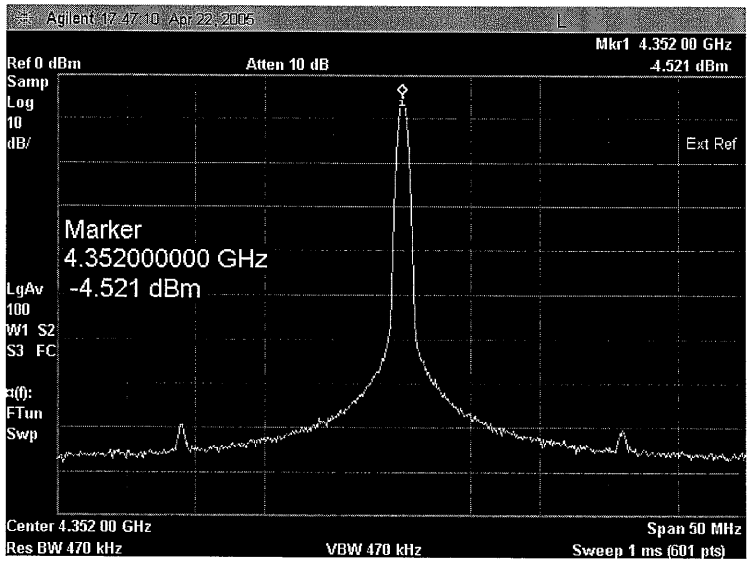


Fig. 4.44 Output frequency spectrum of the proposed frequency synthesizer

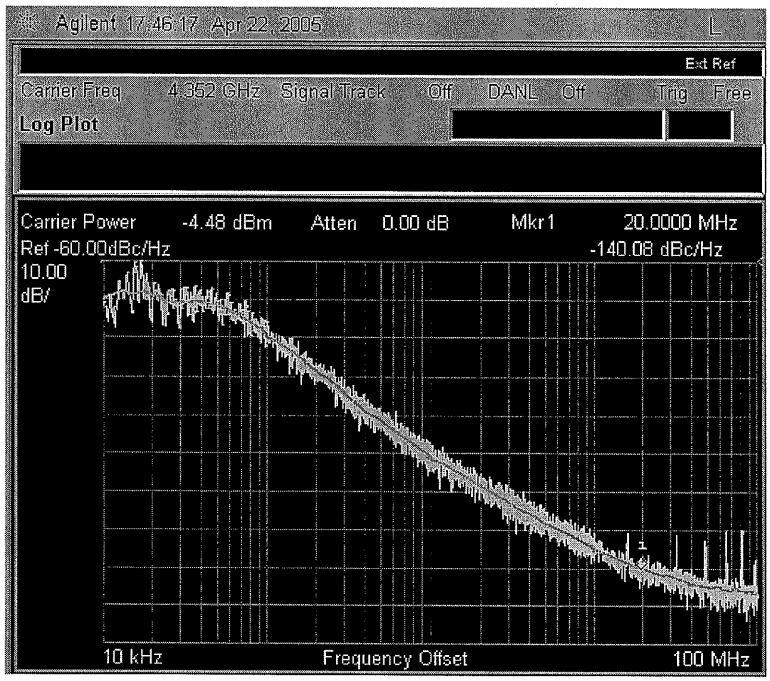


Fig. 4.45 Phase noise plot of the proposed frequency synthesizer

The output waveform for the control voltage of the varactor in the VCO is then obtained by changing the division ratio of the frequency synthesizer. The result is shown in Fig. 4.46. It shows that the settling time is around 86μs.

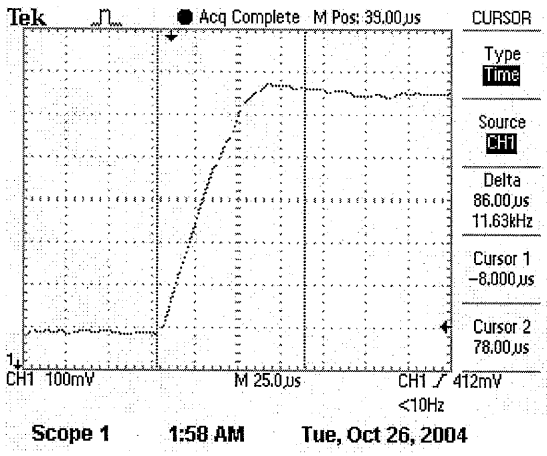


Fig. 4.46 Output waveform of the control voltage for the varactor

All the above measurements are done using a single 1V supply. The total power consumption is only 9.68mW. The performance summary of the frequency synthesizer is listed in Table 4.4.

		Specification	Measurement	
Process		CMOS 0.18μm	CMOS 0.18μm	
Supply voltage /V		1	1	
Reference frequency /MHz		16	16	
Output frequency of LO1 /GHz		4.144-4.256	4.112-4.352	
Output frequency of LO2 /GHz		1.036-1.064	1.028-1.088	
Number of channels		8	16	
Moduli		259-266	257-272	
Phase noise@4.352GHz /dBc/Hz		<-132@20MHz	In-band	-71.1@10kHz
			Out-of-band	-140.1@20MHz
Spur@16MHz		<-57dBm	-75.5 dBc	
Settling time		<100μs	86μs	
Power /mW	VCO+1st divider		5.17	
	2nd divider		2.13	
	3rd divider			
	Other dividers		2.38	
	PFD+CP+LF			
	Total	<10mW	9.68	

Table 4.4 Performance summary of the proposed frequency synthesizer

4.6 Benchmarking

The performance of the proposed frequency synthesizer is compared with that of other published designs in Table 4.5. This work achieves the lowest power consumption and phase noise with only 1V supply.

	[19]	[20]	[21]	[30]	This work
Supply/V	2.5	2.5	1	1.8	1
Process/μm	0.25 CMOS	0.25 CMOS	0.18 CMOS	0.18 CMOS	0.18 CMOS
Frequency/GHz	4.128-4.272	3.2-4GHz	5.45-5.65	5.13-5.44	4.112-4.352
Phase noise /dBc/Hz@20MHz	-138	-136	-137	-136	-140.1
Spurs/dBc	NA	-64	-80 @11MHz	-48 @10MHz	-75.5 @16MHz
Area/mm^2	NA	1.7	0.99	0.43	1.28
Power/mW	180	93	27.5	77	9.68

Table 4.5 Comparison of published frequency synthesizers

[30] occupies the smallest area and uses a 10GHz VCO with its IQ outputs generated at the first-stage frequency divider. All the measurements are obtained at the output of that frequency divider. Yet, the power consumption and the spur are much larger than this design.

In summary, a 1-V CMOS frequency synthesizer for WLAN 802.11a transceivers is successfully demonstrated. A novel transformer-feedback VCO for low voltage and a stacked frequency divider for low power are used to enhance the performance of the synthesizer. It is implemented in a 0.18μm CMOS process. With a 1V supply, the synthesizer measures a phase noise of –140.1 dBc/Hz at an offset of 20 MHz with a center frequency of 4.26 GHz and a frequency tuning range from 4.114 GHz to 4.352 GHz. The synthesizer occupies a chip area of 1.28mm^2 and dissipates only 9.7mW.

Chapter 5 Dual-band VCO with a variable inductor

5.1 Motivation

Frequency tuning mechanisms are required in a wide range of different applications. For example they are required in wireless transceivers for the down conversion of signals at different frequencies, for multiple-band applications and for wide band applications. An ideal frequency tuning circuit will have a wide tuning range, be power efficient and have a high operating frequency.

5.2 Existing solutions

Conventionally a tuning circuit includes an LC tank and a conventional method of providing control of the tuning frequency is by using a variable capacitance such as a varactor to vary the value of C in the LC tank, as shown in Fig. 5.1. Several classes of varactors, such as junction diodes and MOS capacitors, are commonly found. However, this prior art arrangement has the disadvantage that there is a limited frequency range (about 10% only) owing to the limited capacitance ratio of the varactor.

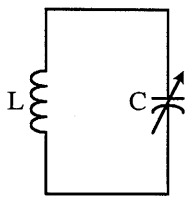


Fig. 5.1 Schematic of a simple LC tank with varactor

Such drawback can be remedied by the use of switched capacitor array (SCA). The maximum capacitance can be obtained by switching on the SCA and the minimum value depends on the parasitic of the switching transistor. Thus, the capacitance ratio can be much larger than that of the varactor.

However, in general, frequency tuning by changing the capacitance of the tank is not energy efficient. This can be illustrated by Fig. 5.2. It shows the impedance of a simple LC resonator when the ratio of the L and C is varied and the resonant frequency is kept unchanged. For such LC resonator, if the value of L increases, the impedance and, also, the quality factor of the tank also increase. Then, less power is dissipated to attain the same output amplitude. In other words, it is more power efficient to minimize the capacitance of the tank and to adjust the inductance for frequency variation. As a result, it is highly desirable to be able to implement integrated variable inductors.

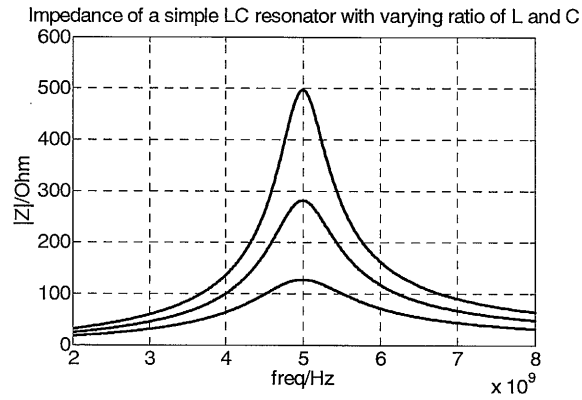


Fig. 5.2 Impedance of a simple LC resonator with varying ratio of L and C

Currently, several techniques are available for providing a variable inductance. These include active inductors and switched resonators. A typical design for an active inductor is the gyrator-C architecture, which employs a gyrator and an integrating capacitor [31]. A gyrator consists of two transconductors connected in a feedback configuration, as shown in Fig. 5.3. This type of active inductor makes use of the parasitic capacitance of the transistors as the integrating capacitor. The inductance of active inductor is:

$$L = \frac{C}{g_{m1} g_{m2}} \tag{5.1}$$

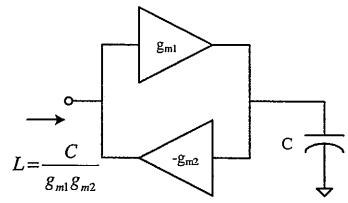


Fig. 5.3 Active inductor

Because only a few active devices are used in this type of inductor, the chip area occupied is usually very small. Tunability is another advantage of this type of active inductor. As shown in the above equation, by changing the bias and, therefore, the transconductance of the transistors, the inductance of the active inductor can be varied.

However, the power consumption and noise contribution of the active devices used in these inductors are generally too high to be practical, and the dynamic range is quite limited. Most important of all, active inductors are generally not suitable for high frequency operation. At high frequencies, the performance of the active inductor is degraded by the phase errors induced by parasitics.

Recently, switched resonators using multiple inductors have been introduced [32][33]. A switched resonator typically comprises two spiral inductors and a switching transistor, either connected in parallel or in series with the inductors as shown in Fig. 5.4. If the switching transistor is connected in parallel with one of the inductors, the inductor is shorted when the switch is on. As a result, the equivalent inductance reduces from L_1+L_2 to L_1.

Fig. 5.4 Switching transistor in series and in parallel

A switched resonator can be used for coarse tuning and another varactor can be used for fine tuning. The tuning range of the resonator can therefore be significantly improved. However, the turn-on resistance of the switching transistor has a great impact on the quality factor of the resonator. It is necessary to increase the size of the transistor in order to reduce the effect of the turn-on resistance on the quality factor. Since the operating frequency of the resonator depends on the equivalent inductance and the capacitance between drain and ground of the switching transistor, the drain capacitance of the switch significantly reduces the operating frequency of the resonator. Thus, this type of switched resonator is not suitable for applications with low noise, low power, and high frequency and requires large chip area for high quality factor.

By mechanically changing the property of some types of resonators, it is also possible to use them for frequency tuning. In [34], the variable inductor consists of a spiral inductor, a conductor plate and a MEMS actuator. The inductance is changed by sliding the conductor plate onto the spiral inductor with different coverage. The conductor plate changes the magnetic flux and, thus, the inductance of the spiral inductor.

However, this is not feasible if the resonator is to be integrated on chip in CMOS process. In addition, the conductor plate sliding onto the inductor induces magnetic loss caused by eddy current. This lowers the quality factor of the inductor. As a result, its measured quality factor in [34] is only 2.5. Much higher consumption is therefore required to start up oscillation and sustain comparable phase noise performance.

5.3 Proposed integrated variable inductor and resonator

5.3.1 Proposed integrated variable inductor

An integrated variable inductor is proposed using an on-chip transformer together with a variable capacitor C_S connected in parallel with the secondary coil as shown in Fig. 5.5.

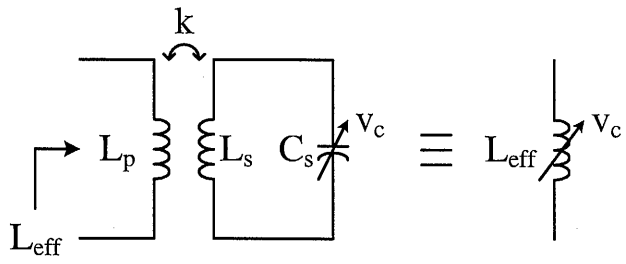


Fig. 5.5 Schematic of the proposed variable inductor

By changing the capacitance C_S, the equivalent inductance looking into the primary coil of the transformer can be tuned. Using a simple T-model for the transformer, as shown in Fig. 5.6, the variable inductance can be derived to be:

$$L_{eff} = L_p + \frac{\omega^2 k^2 L_p L_s C_s}{1 - \omega^2 L_s C_s} \tag{5.2}$$

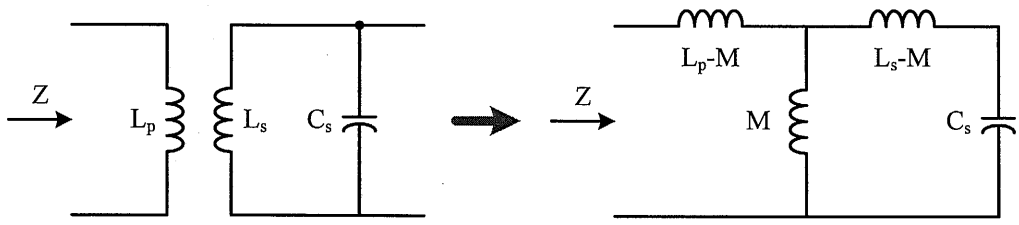


Fig. 5.6 Conversion of the proposed variable inductor using T-model

The effective inductance of the proposed variable inductor as a function of the variable capacitance C_s at a fixed frequency is plotted in Fig. 5.7. With L_p and L_s being 0.8 nH, k being 0.7, and C_s varying from 1 pF to 2 pF, the effective inductance L_{eff} is tuned from 1.2 nH to 8.1 nH corresponding to a tuning range of around 148%.

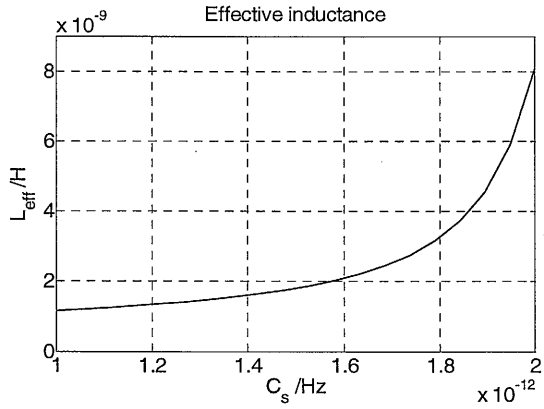


Fig. 5.7 Effective inductance of the proposed variable inductor as a function of C_s

The effective inductance is also a function of frequency. Fig. 5.8 shows the effective inductance as a function of frequency with a particular value of C_s. At very low frequency, the value of the effective inductance gets close to the primary inductance, L_p, whereas, at very high frequency, its value approaches $L_p\left(1-k^2\right)$. This observation can be summarized by the following equations:

$$\begin{cases} \lim\limits_{\omega\to 0} L_{eff} = \lim\limits_{\omega\to 0} L_p + \dfrac{\omega^2 k^2 L_p L_s C_s}{1-\omega^2 L_s C_s} = L_p \\ \lim\limits_{\omega\to \infty} L_{eff} = \lim\limits_{\omega\to \infty} L_p + \dfrac{\omega^2 k^2 L_p L_s C_s}{1-\omega^2 L_s C_s} = L_p\left(1-k^2\right) \end{cases} \tag{5.3}$$

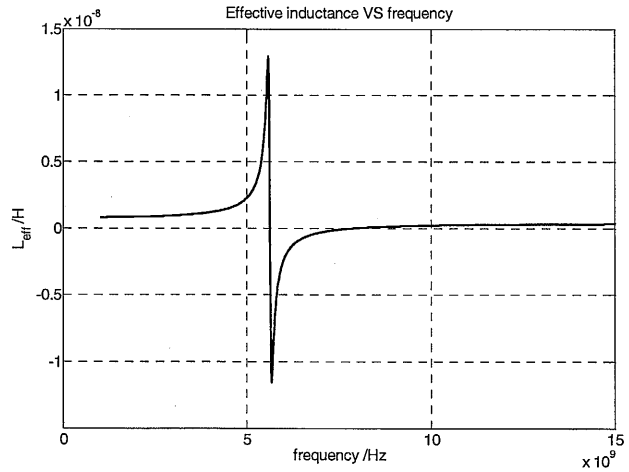


Fig. 5.8 Effective inductance of the proposed variable inductor as a function of frequency

There is a range of frequency in which the effective inductance drops below zero. It is critical to avoid operating the proposed variable inductor in such region. The range of frequency can be derived by the following equation,

$$\begin{aligned} & L_p + \frac{\omega^2 k^2 L_p L_s C_s}{1-\omega^2 L_s C_s} < 0 \\ \Rightarrow & \frac{1}{\sqrt{L_s C_s}} < \omega < \frac{1}{\sqrt{L_s C_s (1-k^2)}} \end{aligned} \tag{5.4}$$

5.3.2 Resonator using the proposed variable inductor

More interestingly, when a fixed capacitor, C_P, is connected in parallel to the proposed variable inductor as shown in Fig. 5.9, the following equation can be derived,

$$\omega^2 = \frac{1}{L_{eff} C_p} \tag{5.5}$$

By substituting equation (5.5) into equation (5.2), the resonant frequency can be represented by the following equation:

$$\omega_0 = \sqrt{\frac{(L_p C_p + L_s C_s) \pm \sqrt{(L_p C_p - L_s C_s)^2 + 4k^2 L_p L_s C_p C_s}}{2 L_p L_s C_p C_s (1-k^2)}} \tag{5.6}$$

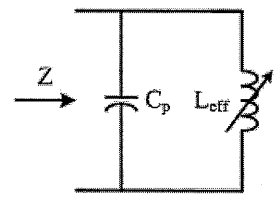


Fig. 5.9 Schematic of the resonator using the proposed variable inductor

Since $(L_p C_p - L_s C_s)^2 + 4k^2 L_p L_s C_p C_s > 0$, there exist inherently 2 distinguished resonant frequencies for any given capacitance C_s. The magnitude of the impedance of the resonator, which exhibits 2 different resonant peaks, is plotted in Fig. 5.10. In

the same figure, the corresponding resonant frequencies at the peaks as a function of the varactor C_s are also plotted. The effective impedances looking into the variable inductor at the 2 resonant frequencies are quite different, and the resonant tank will oscillate at whichever frequency with the higher impedance and the smaller loss. By changing the values of C_s and thus adjusting the maximum values of the effective impedance of the resonator, the oscillation can be switched from one mode to the other. As a result, an oscillator utilizing the resonator can switch between two different frequency bands. If the fixed capacitor at the primary coil C_p is replaced by another varactor, the frequency tuning range can even be extended much further.

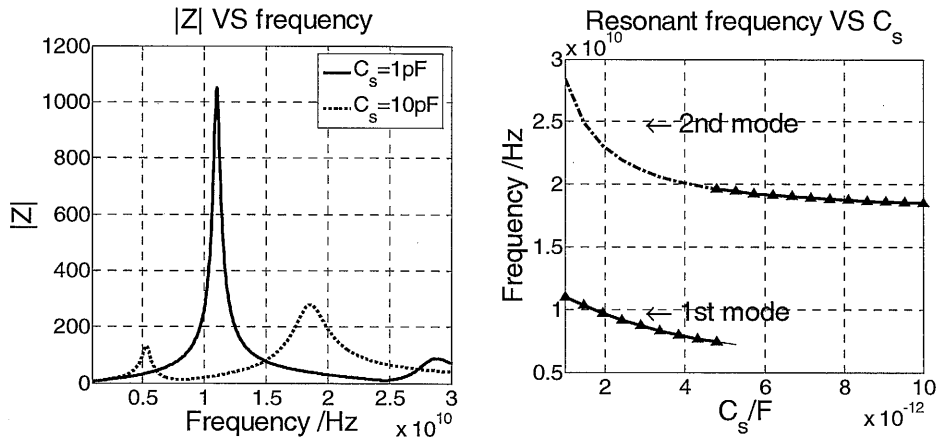


Fig. 5.10 Impedance and resonant frequencies of a resonator using the proposed variable inductor

These properties entail 3 different frequency tuning mechanisms:

1. Frequency tuning in the 1st mode
2. Frequency tuning in the 2nd mode
3. Frequency tuning by switching between the 2 modes

In addition to providing a wide frequency tuning range, due to the isolation of the primary coil from the variable capacitor in the secondary coil, the variable inductor sees a much smaller effective capacitance and can oscillate at a much higher

resonant frequency. In addition, with the coupling between the 2 coils of the transformer, compared to a simple inductor, the quality factor of the variable inductor is improved by (1+k) times, and the parallel impedance of the variable inductor is much larger [35].

5.3.3 Analysis with resistive components

In order to have a study about the impact of non-ideal transformer, resistive components are included into the proposed variable inductor for further analysis. It is assumed that the quality factor of the variable capacitor is negligible and the quality factor of the transformer dominates the loss in the variable inductor. The schematic of the variable inductor with the resistive components is shown in Fig. 5.11. The schematic is then expanded by the equivalent T-model.

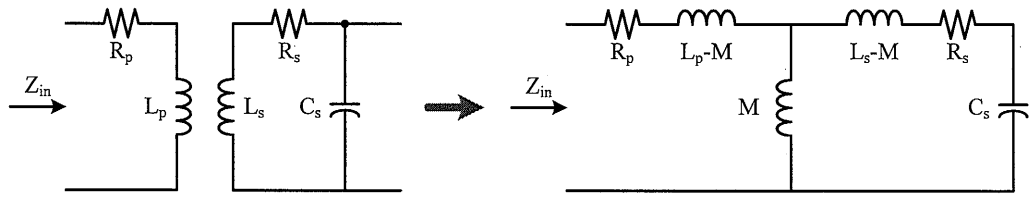


Fig. 5.11 Conversion of the proposed variable inductor with resistive component using T-model

The impedance looking into the schematic can be derived and represented by the following equations:

$$Z_{in} = r_p + s(L_p - M) + sM \left\| \left(r_s + s(L_s - M) + \frac{1}{sC_s} \right) \right. \\ = r_{eff} + sL_{eff} \tag{5.7}$$

where $r_{eff} = r_p + \dfrac{\omega^4 C_s^{\,2} r_s k^2 L_p L_s}{(1-\omega^2 L_s C_s)^2 + \omega^2 C_s^{\,2} r_s^{\,2}}$ (5.8)

and $L_{eff} = L_p + \dfrac{\omega^2 k^2 L_p L_s C_s (1-\omega^2 L_s C_s)}{(1-\omega^2 L_s C_s)^2 + \omega^2 C_s^{\,2} r_s^{\,2}}$ (5.9)

Similar analysis is also applied to the resonator formed by connecting a capacitor, C_p, in parallel with the variable inductor, as shown in Fig. 5.9. For the sake of simplicity, instead of using direct substitution, graphical approach is utilized to derive the resonant frequencies of the resonator with non-ideal components. Equation (5.5), which is used to model the resonator, and equation (5.9), which is used to model the variable inductor with resistive components, are plotted onto the lower part of Fig. 5.12. Different curves, for equation (5.9), are plotted as functions of the frequency and the varactor C_s. There are two intersecting points for each set of curves corresponding to the roots of equations (5.5) and (5.9).

These curves are aligned with the magnitude of the impedance of the resonator with different values of C_s as shown in the upper part of Fig. 5.12. Vertical dash lines, as shown in the figure, can be drawn, passing through the peaks of the magnitude of the impedance, at which the inductive component of the variable inductor cancels exactly with the capacitance, C_s, and the intersecting points of equations (5.5) and (5.9). Thus, it is obvious that the frequencies, at which these intersecting points occur, coincide with the resonant frequencies of the resonator.

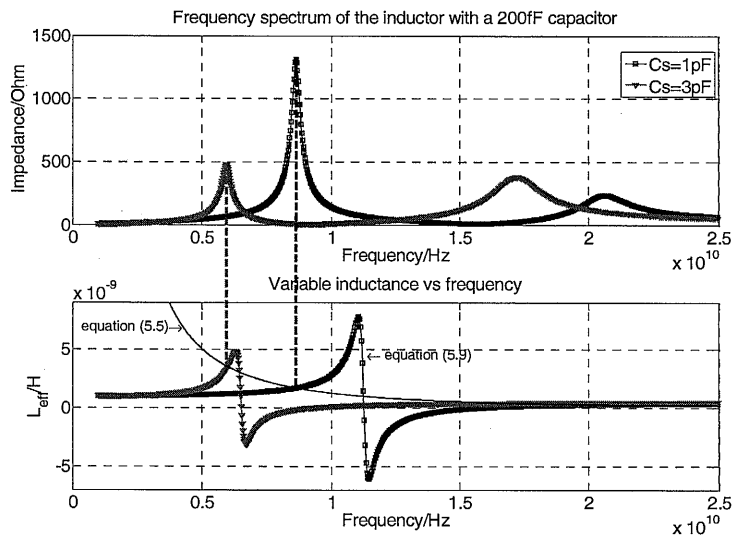


Fig. 5.12 Example of the inductance against frequency

In order to further investigate the impact of the resistive component on the variable inductor, the effective inductance, as a function of frequency, with ideal and non-ideal components are plotted together in Fig. 5.13. As opposed to the analysis with ideal components, the maximum point of L_{eff}, represented by equation (5.9), for any given value of C_s, is no longer infinite and depends on the resistive loss of the inductor and the value of C_s. For some particular values, the peak of L_{eff} drops below equation (5.5) and results in no intersection as shown in Fig. 5.13. Only a single resonant frequency remains in such case. This graphical analysis illustrates that the frequency at which the peak of L_{eff} touches the curve representing equation (5.5), at a single point, is the minimum frequency of the resonator.

The peak of L_{eff} reduces with increasing resistive loss in the variable inductor. Hence one approach to reduce the minimum frequency of the resonator, for a wider frequency tuning range, is to reduce the resistive loss of the variable inductor. This is achievable with the help of simple negative gm cell, which will be shown in later section.

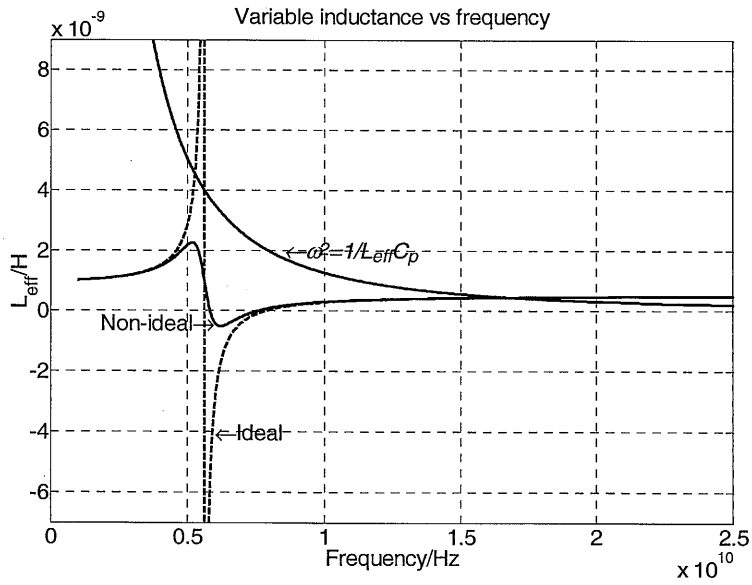


Fig. 5.13 Example of the inductance against frequency

5.3.4 Comparison of the proposed resonator with a simple LC tank

Extensive analysis and simulations have been carried out to verify the advantages of the proposed variable inductor as compared to a simple inductor. In the first comparison, as shown in Fig. 5.14, a 200-fF capacitor is connected in parallel with the primary coil while a 1pF-10pF varactor is connected to the secondary coil. The same capacitor and varactor are connected in parallel to a simple inductor for comparison. The inductance, L_1, in the variable inductor is chosen to be the same as the inductance in the simple LC tank. The effective inductances of both resonators are shown. As shown in Fig. 5.14, the simple LC tank resonates from 1.8 GHz to 5.6 GHz whereas the tank with the variable inductor can oscillate from 5.3 GHz up to 19 GHz (shown in solid line).

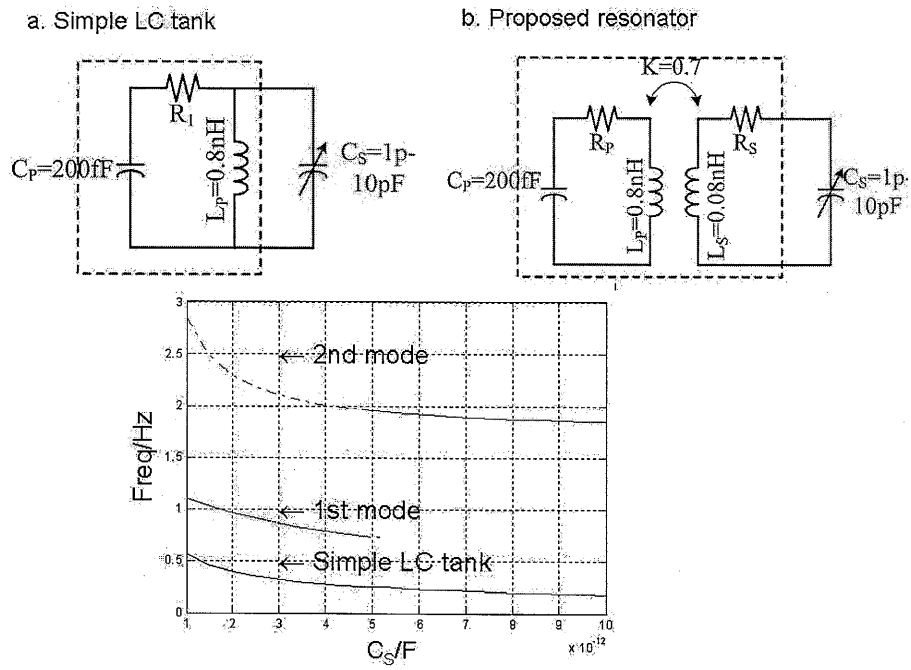


Fig. 5.14 Comparison of resonant frequency of (a) simple LC tank and (b) proposed resonator for the same L and C

In the second study, the varactor in the simple LC tank is reduced by four times, as shown in Fig. 5.15. The fact that the two circuits achieve similar resonant

frequencies verifies the capability of the proposed variable inductor to operate at the same frequency for a much larger varactor and thus for a much wider tuning range as compared to a simple inductor. Moreover, the magnitude of the simple resonant tank is still only 70% of the tank with the variable inductor. At 11.2 GHz, the Q of the tank with the variable inductor is 11.4 whereas the Q of the simple LC tank is only 7.4.

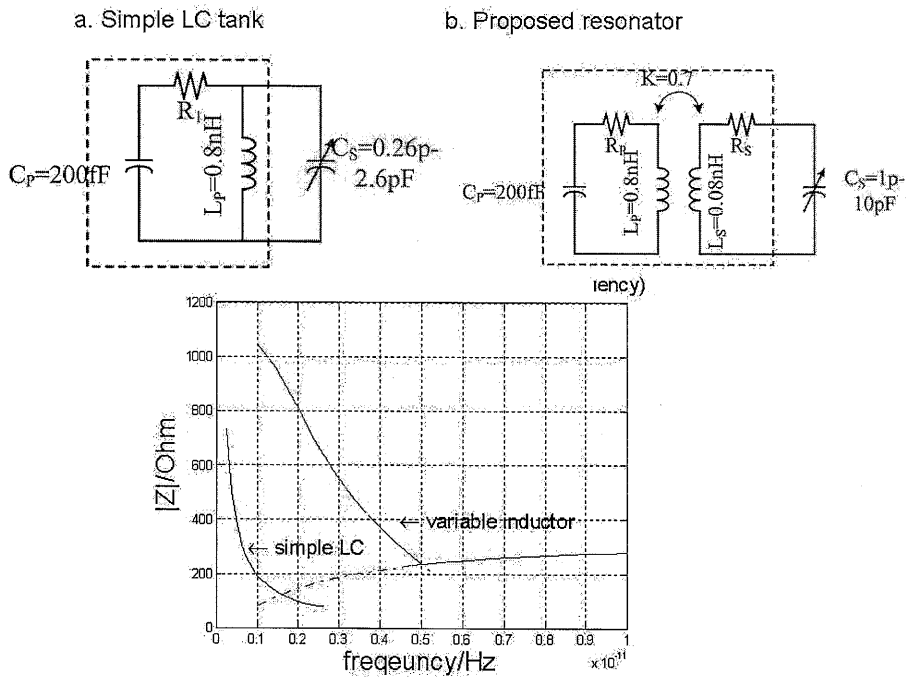


Fig. 5.15 Comparison of parallel impedance of (a) simple LC tank and (b) proposed resonator at the same resonant frequencies

Therefore, it can be concluded that a resonator using the proposed variable inductor can oscillate at much higher frequencies with a much larger frequency tuning range than a simple LC tank with the same varactor and the fixed capacitor. Moreover, a resonator using the proposed variable inductor with the transformer's coupling coefficient, *k*, indeed achieves an equivalent quality factor approximately *(1+k)* times better than that of a simple LC tank with the same inductance.

5.4 Design of a VCO with the proposed variable inductor

5.4.1 VCO Core

The proposed variable inductor is demonstrated by integration with a voltage-controlled oscillator for dual-band applications as shown in Fig. 5.16. The VCO has a differential configuration with a single 4-port center-tapped symmetrical transformer.

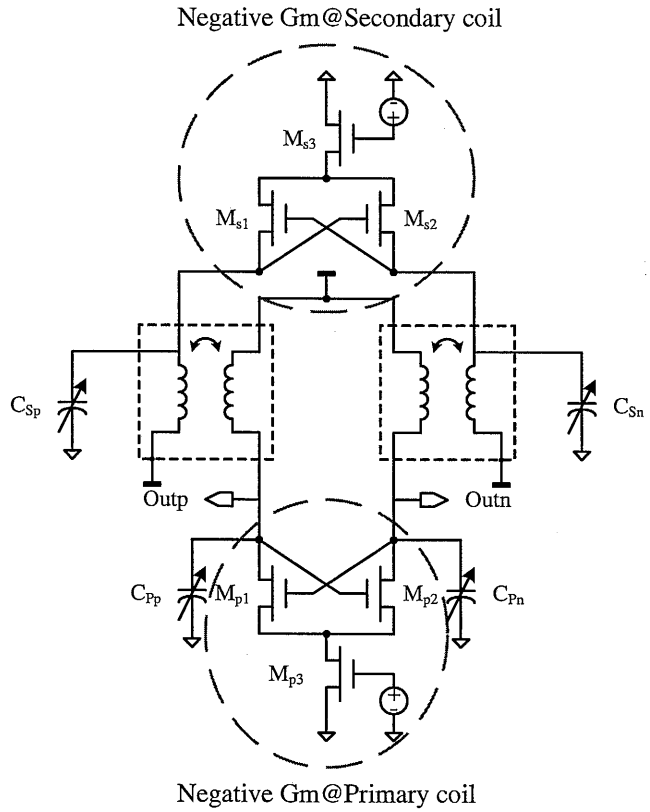


Fig. 5.16 Schematic of the proposed dual-band VCO

5.4.2 Transformer

The 4-port on-chip transformer, shown in Fig. 5.17, is realized with 2 planar symmetrical coils. The parameters, L_p, L_s and k are obtained by optimization for the specified resonant frequencies. The length and number of turns for each coil are first determined by using *ASITIC* [36].The 2 coils are combined and interleaved between each other in order to increase their magnetic coupling. The final transformer is

simulated in *MOMENTUM*. The simulated S-parameters are used for fitting in a wide-band transformer model, as shown in Fig. 5.18, for later simulation with the active circuit in *Analog Artist*.

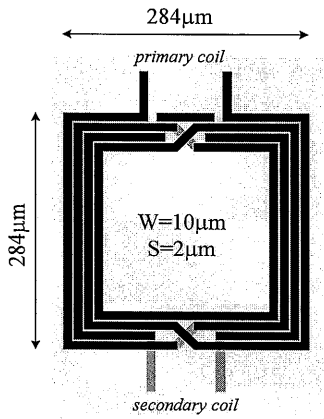


Fig. 5.17 Physical layout of the 4-port differential transformer

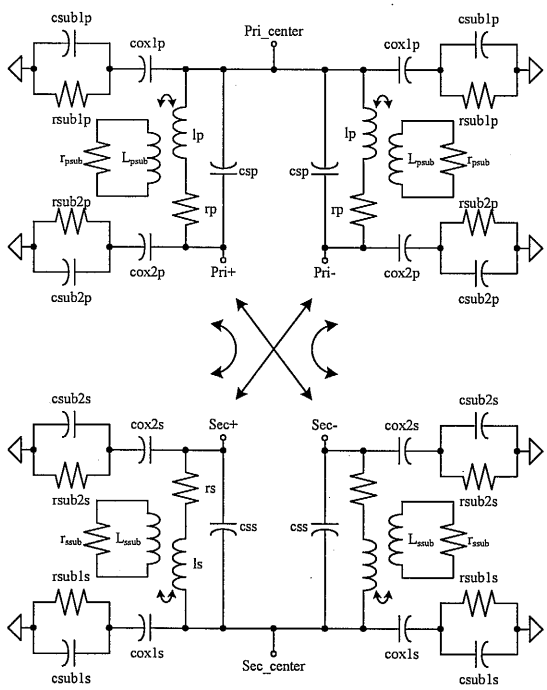


Fig. 5.18 Schematic of the wide-band transformer model

Due to its differential configuration, the on-chip transformer combines the four coils required in a differential variable inductor into one. It occupies only $0.28\times0.28mm^2$, which saves much area as compared to using 2 identical

singled-ended transformers. Both the primary and the secondary coils have center taps as common nodes. The primary and secondary ports are placed on opposite sides of the transformer. This allows the SCAs, the negative gm cells, and the buffer to be laid out on different sides of the transformer to achieve better symmetry and smaller parasitics due to shorter metal connections

5.4.3 Variable capacitors

For demonstration, the variable capacitors C_p and C_s in the primary and secondary coils are implemented with switched capacitor arrays (SCAs) respectively. The schematic of an N-bit SCA is shown in Fig. 5.19. The parameters in the SCA are determined by the desired tuning range and quality factor of the SCA.

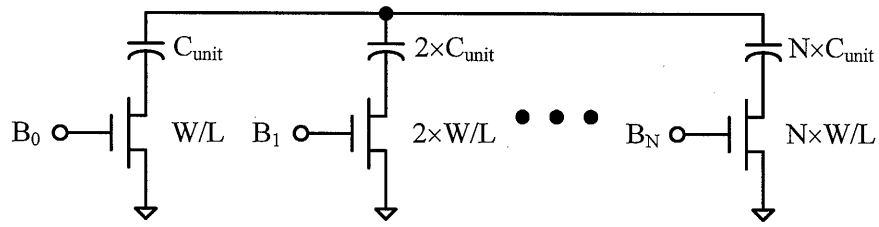


Fig. 5.19 Schematic of the SCA

One way to optimize the tuning range is to reduce the drain area and, thus, its parasitic capacitance by utilizing doughnut transistors for the SCA. Its layout is shown in Fig. 5.20. Instead of using a finger-type layout, the gate is bent to form a square. The drain diffusion is then surrounded by the gate and the source diffusion. By sharing the drain diffusion in this way, the effective width to drain capacitance ratio is increased. For the source diffusion, since it is connected to the ground, the increase in the source area is not detrimental to the design. In order to maximize the effective width to drain capacitance ratio, the smallest area allowable in the process is used. This fixes the width of each doughnut transistor. But the width of the NMOS switch can be increased by connecting all these units in parallel.

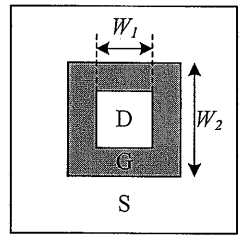


Fig. 5.20 Layout of the doughnut transistor

A rough estimation of the effective width of the doughnut transistor is the average of the inner and outer perimeter of the gate width. For more accurate analysis, the following equation derived in [37] can be used,

$$\left[\frac{W}{L}\right]_{eff} = 2n\frac{\tan(\pi/n)}{\ln(W_2/W_1)} \tag{5.10}$$

where n is the number of side of a doughnut transistor

In the case of a rectangular-shaped doughnut transistor, n is simply equal to 4.

C_s and C_p in the variable inductor are implemented using binary-weighted 2-bit and 5-bit SCAs. By changing the values of C_s, the 2 inherent resonant frequencies as well as the maximum values of the impedance in each mode, can be adjusted, as mentioned previously. When C_s increases beyond a particular value, there is a swap in the maximum value of the impedance. Since oscillation starts at the frequency with the higher quality factor, which requires less energy to trigger oscillation, the oscillator can then switch from one mode of oscillation to another.

5.4.4 Negative gm cell

A simple negative gm cell, M_{p1}-M_{p3}, is added in parallel with the variable inductor to cancel the resistive component of the resonant tank to start up and maintain oscillation in the VCO.

The differential signal swing at the outputs of the VCO is equivalent to the gate-drain voltage across the transistors in the negative gm cell. Because the differential signal swing is larger than the threshold voltage, the transistors in the negative gm cell go into the linear region, at a particular point of every oscillation cycle. If the common node of the NMOS negative gm cell is connected to ground directly, the momentarily small transconductance given by those transistors in the linear region reduces the average impedance of the resonant tank. Current sources, always working in the saturation region, are used to bias the negative gm cell to prevent this problem [38]. Since the impedance looking into these current sources is large they can help to remedy this problem by preventing the negative gm cell from reducing the quality factor of the resonant tank.

As mentioned in Section 5.3, the minimum frequency in the first mode increases with the resistive loss of the variable inductor. By reducing the resistive loss of the secondary coil, the minimum frequency for the first mode of oscillation can be reduced, without affecting the maximum frequency for the first mode much. This is achieved by connecting a second negative gm cell, M_{s1}-M_{s3}, as shown in Fig. 5.16, in parallel with the differential secondary coil. With the same argument used for the negative gm cell in the primary coil, a current source implemented by a single MOS, M_{s3}, is added in series at the common node of the negative gm cell.

5.4.5 Automatic amplitude control block

An automatic-amplitude-control (AAC) loop is integrated into the proposed VCO to provide constant output amplitude for different frequencies. The AAC block consists of a peak detector, an error amplifier, and a low-pass filter. The output of the VCO is rectified and low-pass filtered by the peak detector. The filtered signal is then compared with a reference voltage by the error amplifier. The amplifier's output

is used to regulate the tail current source of the VCO, which is designed to operate within the current-limited regime.

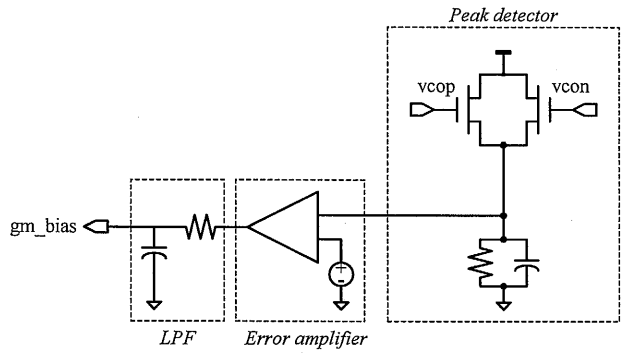


Fig. 5.21 Schematic of the AAC block

5.5 Experimental results

The proposed VCO is implemented in a TSMC 0.18μm CMOS process (V_{Tn} = 0.52 V, V_{Tp} = - 0.54 V). Fig. 5.22 shows the die micrograph of the VCO, which occupies a chip area of 0.4×0.8mm^2.

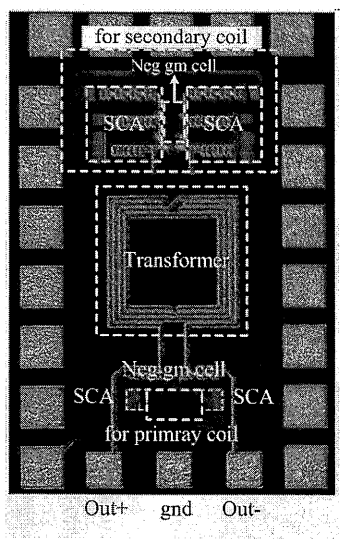


Fig. 5.22 Die micrograph of the proposed VCO

5.5.1 Transformer

A separate testing structure for the transformer is measured by the network analyzer. Calibration structures, including open and shorted pads, are also measured.

S-parameters after pad de-embedding, shown in Fig. 5.23, are used for model fitting. The measured inductances and Q's for the primary and the secondary coils are 0.92 nH, 6.3, 0.87 nH, and 6, respectively. The measured coupling factor is 0.74, which is very similar to the simulated value.

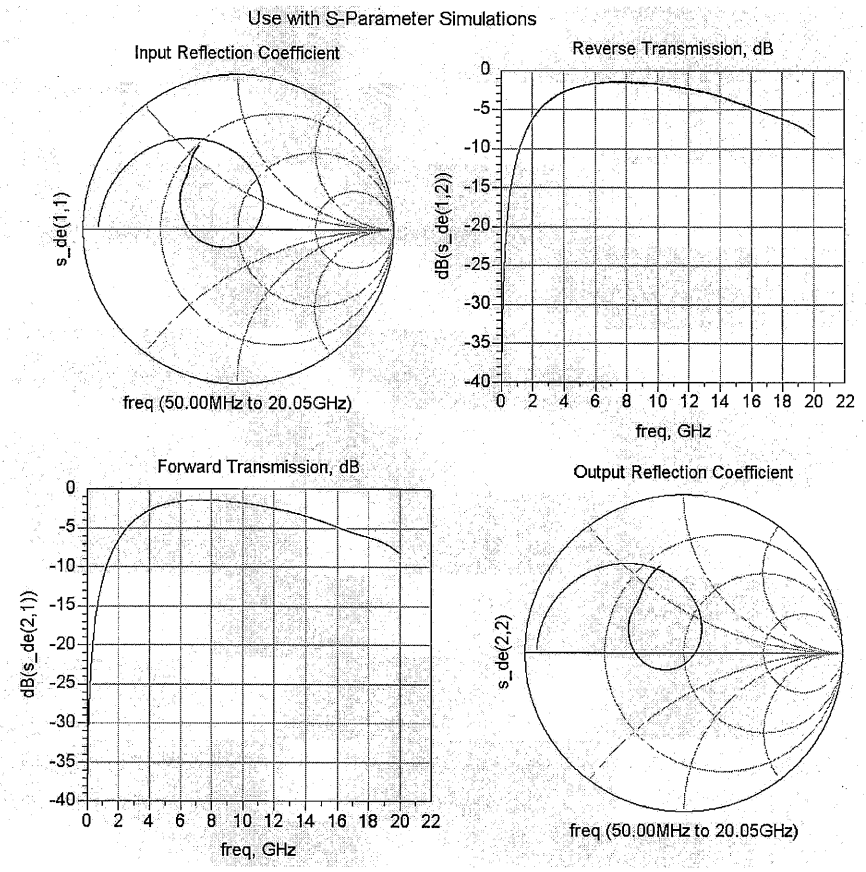


Fig. 5.23 Measured S-parameters of the transformer after pad de-embedding

5.5.2 SCA

A separate testing structure for a unit cell of the SCA is also measured by the network analyzer. After pad de-embedding, the measured S-parameters are shown in Fig. 5.24. The quality factor and capacitance of the SCA when it is turned on is shown in Fig. 5.25. The minimum Q achieved at the highest oscillation frequency of the VCO is 15.5. The minimum capacitance achieved by a unit cell of the SCA is 263fF. It is quite constant across the whole frequency tuning range of the VCO.

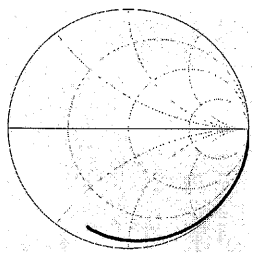


Fig. 5.24 Measured S-parameters of the SCA

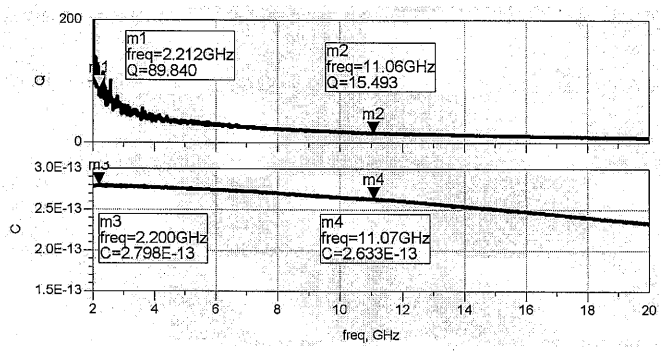


Fig. 5.25 Measured quality factor and capacitance of the SCA in ON state

5.5.3 VCO

The measured frequency spectrums for the two different bands are shown in Fig. 5.26, as measured by Agilent E4440A at the output of the on-chip open-drain buffer. The measured frequencies range from 2.2GHz to 3.6GHz and 10.7GHz to 11.3 GHz for the lower and upper bands respectively. With the AAC being turned on, the output power at the open-drain buffer of the VCO remains constant for both bands at around -12dBm, as shown in Fig. 5.27.

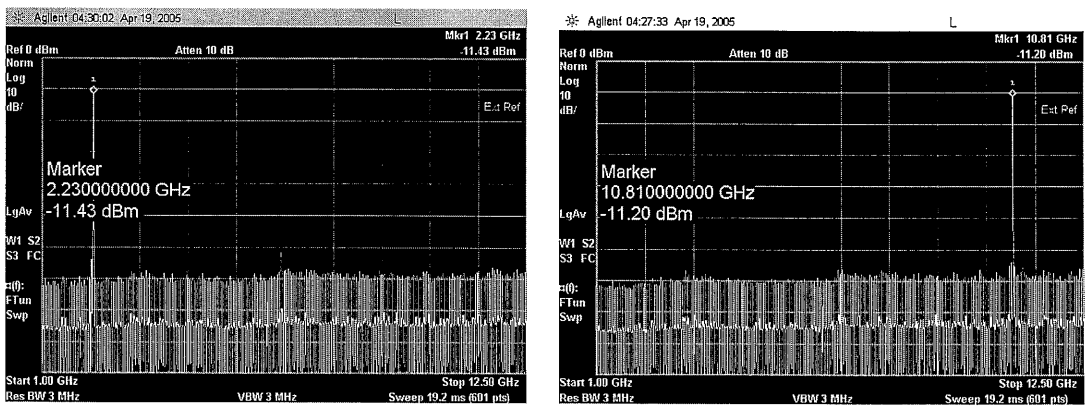


Fig. 5.26 Measured frequency spectrum of the proposed VCO

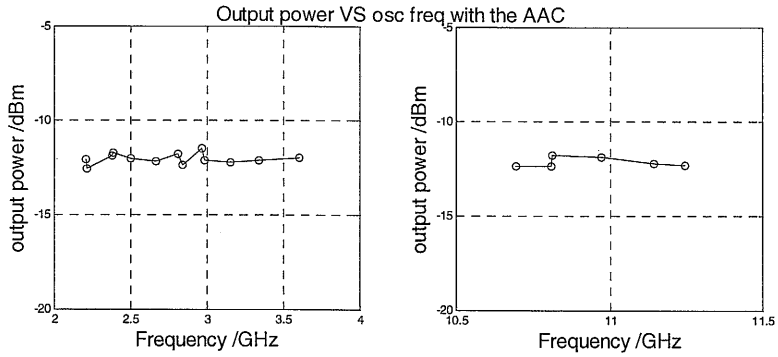


Fig. 5.27 Output power of the proposed VCO with AAC

As shown in Fig. 5.28 and Fig. 5.29, at 1V, the VCO measures a phase noise of around -118.2 dBc/Hz and -110.1dBc/Hz at 1-MHz offset for the lower and upper bands respectively. The corresponding FOMs are Fig. 5.30 plots the phase noise and power consumption as functions of oscillation frequency. Table 5.1 summarizes the measured performance.

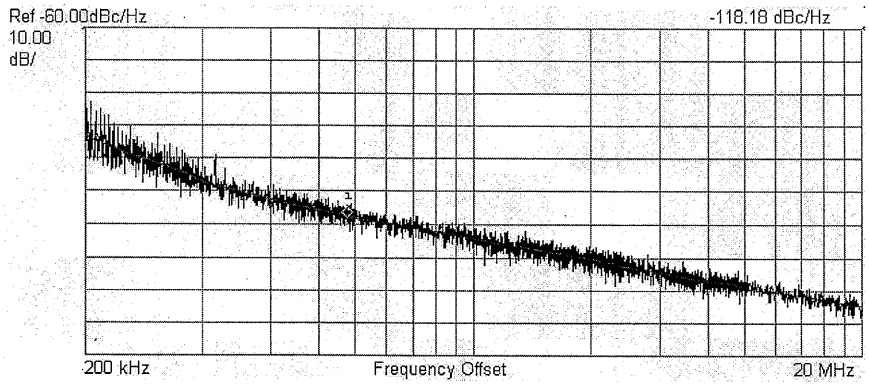


Fig. 5.28 Phase noise plot of the proposed VCO for the lower band

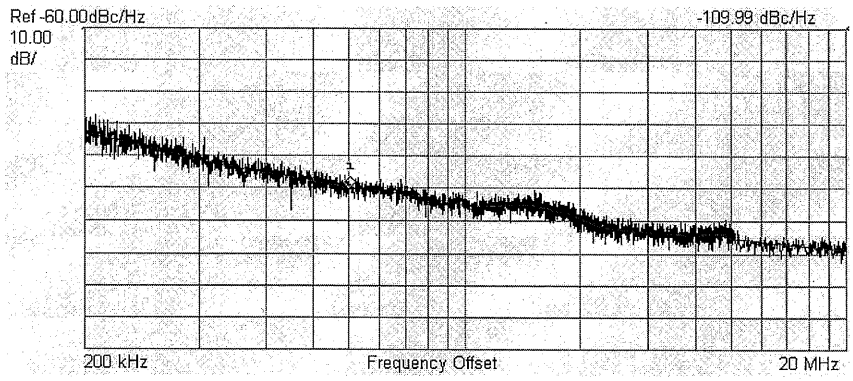


Fig. 5.29 Phase noise plot of the proposed VCO for the upper band

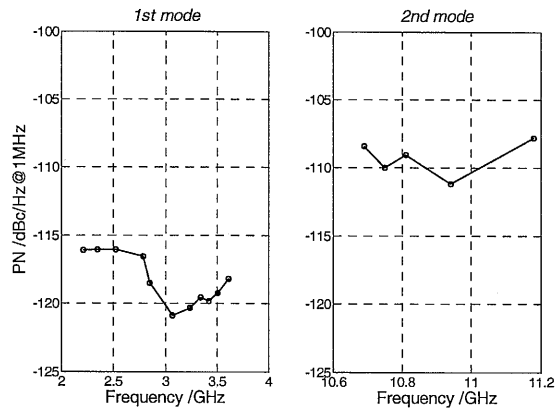


Fig. 5.30 Measured phase noise of the proposed VCO as a function of frequency

	Lower band	Upper band
Process	TSMC 0.18μm	
Supply Voltage	1V	
Frequency /GHz	2.2-3.6	10.7-11.3
Output power /dBm	-12 (with the AAC turned on)	
Power consumption /mW	3.8-9.4	3.5-4.9
Phase noise /dBc@1MHz	-116 – -120.9	-108.2 – -111.2

Table 5.1 Performance summary of the proposed VCO

Table 5.2 shows the table of comparison of the proposed VCO with some published dual-band and wide-band VCOs. The proposed VCO can operate with the highest frequency and the largest tuning range for the two bands.

Reference		[33]	[39]	This work
Process		CMOS 0.18μm	CMOS SOI 0.13μm	CMOS 0.18μm
Supply/V		1	1	1
f;ow/GHz		2.4-2.52 (5%)	3.8-5.7 (40%)	2.2-3.6 (48%)
fhigh/GHz		4.65-5.12 (10%)		10.7-11.3 (5%)
Power /mW	low band	4.6	2.3	3.8-9.4
	high band	6		3.5-4.9
L{f} /dBc/Hz @1MHz	low band	-132 – -134	-121.7	-116.0 – -120.9
	high band	-125 – -126		-108.2 – -111.2
Chip Area		0.8×0.8mm^2	0.46×0.64mm^2	0.4×0.8mm^2

Table 5.2 Table of comparison with recently published VCO

In summary, further development on the design of VCO is studied. An integrated variable inductor is proposed and analyzed. A dual-band VCO, employing such an integrated variable inductor, is demonstrated to oscillate from 2.2GHz to 3.6GHz in the lower band and 10.7GHz to 11.3GHZ in the upper band at a 1-V supply using a 0.18μm CMOS process. The values of phase noise are -118.2 dBc/Hz for the lower band and -110.0dBc/Hz for the upper band at 1-MHz offset while consuming 5mW. The AAC of the proposed VCO is also demonstrated. The proposed VCO, can thus, be used to generate constant output power for the two different frequency bands.

Chapter 6 Specifications of the building blocks in the transceiver

6.1 Building blocks in the receiver

6.1.1 Low noise amplifier

From the above equation, it is obvious that the noise figure of the LNA dominates the noise performance of the whole receiver. The target noise figure is set to be 4dB.

Power gain of the LNA needs to be sufficiently large to amplify the input signal to compensate for the noise degradation contributed by the following stages. The ultimate target is to attain the required signal-to-noise ratio, specified in the standard, at the output of the receiver. A noise figure achievable by the down-conversion mixer is around 12dB. Therefore, the gain of the LNA has to be, at least, larger than 12dB.

However, its gain cannot be too large so as to ensure that, at least, the down-conversion mixer is not saturated and the linearity of the whole receiver is good enough. As mentioned in Chapter 3, the maximum input power to the LNA including the effect of PAPR, is -24dBm. By assuming that the 1dB compression point of the mixer is -5dBm, the maximum gain of the LNA should not exceed 19dB. The target power gain of the LNA is set to be 16dB, which corresponds to a voltage gain of around 23dB. A gain range of around 5dB is also included to accommodate different levels of input power so that the linearity of the mixer can be relaxed.

Its 1dB compression point has to be larger than the maximum input power, which is -24dBm. Thus, the IIP3 required should be larger than -14dBm, assuming a 10dB difference between IIP3 and 1dB compression point.

The input frequency for the LNA is 5.15-5.35GHz, corresponding to a minimum input and output bandwidth of 200MHz. Input matching of the receiver is totally dependent on the LNA. A value of S_{11} less than -10dBm is typically required for the LNA for acceptable input matching within the aforementioned bandwidth.

6.1.2 Down-conversion mixer

As mentioned in Chapter 2, the cascaded out-of-channel IP3 of the receiver is,

$$\frac{1}{IP3_{total}^{\ 2}} = \frac{1}{IP3_{LNA}^{\ 2}} + \frac{A_{v,LNA}^{\ 2}}{IP3_{mixer}^{\ 2}} + \frac{A_{v,LNA}^{\ 2} A_{v,mixer}^{\ 2}}{IP3_{filter}^{\ 2} L_{mixer}^{\ 2}} + \frac{A_{v,LNA}^{\ 2} A_{v,mixer}^{\ 2} A_{v,filter}^{\ 2}}{IP3_{VGA}^{\ 2} L_{filter}^{\ 2}} \quad (6.1)$$

The selectivity at the output of the down-conversion mixer and the channel-selection filter help to reduce the IM3 products of the interferer present at the input. By implementing sufficient attenuation in the adjacent channels, the contribution of the 3rd and 4th terms in the above equation can be minimized. In other words, the IP3 of the receiver is dominated by the 2nd term, including the effect of the LNA gain and the IP3 of the mixer. Since the target voltage gain of the LNA is 23dB, the IP3 of the mixer is set to be around -5dBV to attain an IP3 of -28dBV for the whole receiver. The pass-band voltage gain of the mixer is 0dBV.

The input frequency starts from 5.15GHz to 5.35GHz. After two down-conversion, the maximum output IF frequency is 10MHz. In order to diminish the effect of the 3rd and 4th term in the above equation, the attenuation of the mixer at 40MHz, which is 2 channel bandwidth away from the edge of the IF channel, is set to be 12dB. This can be easily achieved by using a first-order RC low-pass filter at

the output of the mixer. The target pass-band voltage gain of the mixer is set to be 0dB to ensure that the amplified signal does not saturate the filter.

6.1.3 Channel-selection filter

The channel-selection filter has a band-pass characteristic. It has to filter out the DC components and the interferers outside the desired channel. It also acts as an anti-aliasing filter for the ADC. Since the frequency of the zero subcarrier starts from -156kHz to +156kHz, the lower 3dB corner is set to be 100kHz. The occupied bandwidth of the desired channel is 16.6MHz. Therefore, the upper 3dB corner should be, at least, half of the channel bandwidth. It is set to be 10MHz.

It is critical for the channel-selection filter to provide sufficient filtering so that the power level of the adjacent channel interferers at the output is smaller than the total output noise of the receiver. This helps to avoid degradation in the sensitivity of the receiver and relax the required dynamic range of the ADC. The relationship among the power level of the interferer, selectivity of the channel-selection filter and the output noise of the receiver [40] can be written as,

$$\begin{aligned} & P_{\text{int}} - S_{mixer} - S_{filter} \le P_{out,noise} \\ \Rightarrow\ & P_{\text{int}} - S_{mixer} - S_{filter} \le P_{in,noise} + NF \\ \Rightarrow\ & P_{\text{int}} - S_{mixer} - S_{filter} \le (-174 + 10\log BW) + NF \end{aligned} \tag{6.2}$$

where P_{int} is the power level of the interferer and S_{block} is the selectivity or attenuation provided by a building block

The specified adjacent and alternate adjacent channel rejection is -1dB and 15dB respectively. For a modulation of QAM-64, the minimum input power level is -65dBm. This implies that the power levels of the interferers at the adjacent and alternate adjacent channels are -66dBm and -50dBm at the antenna. By assuming a 3dB drop in the antenna, the target selectivity of the filter at 20MHz and 40MHz are,

$$\begin{cases} -66-3-6-S_{@20MHz} \le (-174+10\log 16.6M)+10 \\ -50-3-12-S_{@40MHz} \le (-174+10\log 16.6M)+10 \end{cases} \Rightarrow \begin{cases} S_{@20MHz} \ge 16.8dB \\ S_{@40MHz} \ge 26.8dB \end{cases} \quad (6.3)$$

An attenuation of 30dB at DC should be sufficient to eliminate the DC offset. Its pass-band gain is set to be 10dB with a noise figure of 20dB. Its target IP3 is -10dBV.

6.1.4 Variable gain amplifier

The input power level to the receiver varies from -82dBm, which is the sensitivity for a data rate of 6Mb/s, to -30dBm, which is the specified maximum input power. As mentioned in Chapter 3, the corresponding voltage gain of the receiver varies from 34dB to 86dB. Since the cascaded voltage gain of the LNA, down-conversion mixer and channel-selection filter is 33dB, the target voltage gain of the VGA starts from 1dB to 53dB with continuous tuning capability. The target noise figure and IP3 are 20dB and -13dBV. The target lower and corner frequencies are 100kHz and 25MHz respectively.

6.1.5 ADC

The dynamic range requirement for the ADC is defined as [40],

$$DR = P_{\text{int,max}} - S - (P_{in,\text{min}} - SNR) \quad (6.4)$$

where $P_{int,max}$ is the maximum interferer, S is the selectivity of the receiver, $P_{in,min}$ is the minimum input power and SNR is the signal-to-noise ratio of the receiver

It is assumed that, in the worst-case scenario, the maximum power level of the interferer is -30dBm at the adjacent channel. For a rate of 54Mb/s, the SNR required is 18.4dB with a minimum input power of -65dBm. As mentioned in the previous

section, the selectivity specified is 22.8dB for the whole receiver. Thus, the required dynamic range of the ADC is 30.6dB. Its number of bits required is [41],

$$N = \frac{DR - 1.76}{6.02} = \frac{30.6 - 1.76}{6.02} = 4.8 \tag{6.5}$$

Therefore, an ADC with a resolution of, at least, 5 bits are required. By taking into account the non-idealities of the receiver and the ADC, 3 more bits are added as margin. An 8-bit ADC is to be implemented. The maximum input frequency is 10MHz and the sampling frequency is set to be 40MHz.

The specifications for each building block are summarized in Table 6.1.

	LNA	Dn-mx	CSF	VGA	Total
					
Individual voltage gain W/L (dB)	23.0	0.0	10.0	63.0	96.0
Individual IIP3 (dBV)	-15.0	-5.0	-10.0	-13.0	
Cascaded IIP3 (dBV)	-15.0	-28.2	-29.4	-29.4	-29.4
Noise Fig. (@50, dB)	4.0	13.0	23.0	15.0	
Cascaded Noise Fig. (dB)	4.00	4.27	7.95	7.99	7.99

Table 6.1 Summary of the specification for each building block

6.2 Building blocks in the transmitter

6.2.1 DAC

Similar to the specification of the ADC, the resolution of the DAC required is 8 bits. The maximum input frequency is 10MHz and the sampling frequency is set to be 40MHz.

6.2.2 Filter

Because there is no adjacent channel interferer at the output of the DAC, the filter in the transmitter acts only as an anti-aliasing filter. It also helps to reject the

DC components, located within the zero sub-carrier of the DAC. The required cutoff frequencies are 100kHz and 10MHz. The attenuation at 40MHz should be larger than 10dB. Since the attenuation requirement is quite relaxed, only passive filter is needed. Linearity is not a problem for passive filter and the pass-band loss is expected to be around 3dB.

6.2.3 Up-conversion mixer

The maximum input frequency of the up-conversion mixer is 10MHz. The input signal is then up-converted twice to an output frequency of 5.2GHz. The amplitude of the input signal from the DAC cannot be too small in order to preserve its SNR. This increases the linearity requirement of the mixer. In addition to this, its conversion gain cannot be too small to avoid deteriorating the gain of the whole transmitter. Optimization of the linearity and conversion gain is done together with the PA. The results will be shown in the next section. Single sideband rejection and LO leakage of the mixer should be larger than 30dBc and smaller than 20dBc respectively.

6.2.4 Power amplifier

As mentioned in Chapter 3, an output power of 16dBm is too large for an on-chip PA operating under 1-V supply. The on-chip PA is therefore used as a pre-amplifier, instead. Its target output power is reduced to $0.6V_{pp}$, which is equivalent to -13dBV or 0dBm. An external power amplifier is connected at the output of the on-chip PA to boost the gain to generate an output power of 16dBm. This implies that the output-referred 1dB compression point of the on-chip PA has to be larger than 0dBm.

Some iterations are done among linearity and conversion gain of the mixer and PA. The results are shown in Table 6.2. The output-referred 1dB compression point

of the mixer and PA are -16dBV and -5dBV with voltage gain of 4dB and 10dB. The cascaded 1dB compression point complies with the system specification of the transmitter mentioned in Chapter 3.

	Filter	Mixer	PA
			
Individual voltage gain W/L (dB)	-3.0	4.0	10.0
Individual IIP3 (dBV)		-8.0	-6.0
Cascaded IIP3 (dBV)		-5.0	-9.1
Individual output P_{1dB} (dBV)		-14.0	-6.0
Cascaded output P1dB (dBV)		-14.0	-8.1

Table 6.2 Summary of the specification for each building block

The specification of each building block is summarized in Table 6.3.

LNA	
Input/output frequency	5.15-5.35GHz
Power gain	16dB with 5dB variable gain
IIP3	>-14dBm
Noise figure	<4dB
S11	<-10dB
Down-conversion mixer	
Input frequency	4.144-4.256GHz
Output frequency	0-10MHz
Voltage gain	0dB
IIP3	>-5dBV
Noise figure	<12dB
LO signal	$<0.4V_{pp}$
Output attenuation at 40MHz	12dB
Channel-selection filter	
Lower/upper 3dB frequencies	100kHz/10MHz
Pass-band voltage gain	10dB
IIP3	>-10dBV
Noise figure	20dB
Stop-band attenuation	16.8@20MHz
	26.8@40MHz
VGA	
Lower/upper 3dB frequencies	100kHz/30MHz
Pass-band voltage gain	1-53dB
IIP3	>-13dBV
Noise figure	15dB
ADC	
Input frequency	0-10MHz
Sampling frequency	40MHz
Dynamic range	>30.2dB
Resolution	8 bits
Optimum input voltage	$0.5V_{pp}$ (single-ended)
DAC	
Input frequency	0-10MHz
Sampling frequency	40MHz
Resolution	8 bits
Up-conversion mixer	
Input frequency	0-10MHz
Output frequency	4.144-4.256GHz
Voltage gain	4dB
IIP3	>-14dBV
LO signal	$<0.4V_{pp}$
Power Amplifier	
Frequency Band	5.15-5.35GHz
Output power	>0dBm
Output P_{1dB}	-5dBV
Spectrum mask	-20 dBr @ f_{offset}=9Mhz
	-28 dBr @ f_{offset}=11Mhz
	-40dBr@f_{offset}=20Mhz

Table 6.3 Summary of the specification for the proposed transceiver

6.3 Circuit description of the building blocks in the receiver

6.3.1 LNA

A cascode structure with inductive degeneration is utilized in the LNA. Its half-circuit schematic is shown in Fig. 6.1. The cascode transistor, M_2, increases the reverse isolation of the circuit, which also helps to enhance its stability. 50Ω matching is achieved by the use of inductive degeneration. The input impedance of the LNA can be written mathematically as,

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \frac{g_{m1}}{C_{gs}} L_s \tag{6.6}$$

Real components in the equation remain when the imaginary parts cancel with each other. Hence, 50Ω matching is attained when,

$$\begin{cases} \omega(L_g + L_s) - \dfrac{1}{\omega C_{gs}} = 0 \\ \dfrac{g_{m1}}{C_{gs}} L_s = 50 \end{cases} \tag{6.7}$$

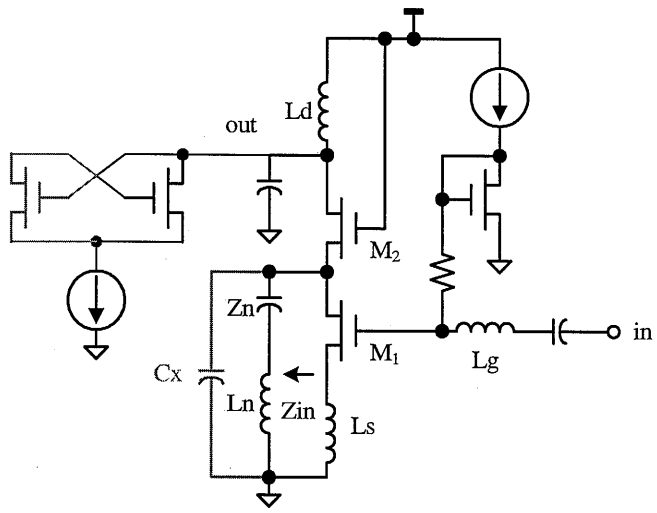


Fig. 6.1 Half circuit of the LNA

Problem caused by the image signal is insignificant in the topology chosen for the proposed receiver assuming that the image signal, 4.2GHz, is far away from the desired RF frequency, 5.25GHz, so that the attenuation at the image frequency is large. The LC tank at the output of the LNA attenuates part of the image signal. With the addition of a notch filter at the output of the LNA, attenuation at the image frequency is further increased before the first-stage down-conversion. The above assumption can be fully realized.

As shown in Fig. 6.1, the notch filter is composed of L_n, C_n and the parasitic C_x. The impedance looking into the notch filter is,

$$Z_n(s) = \frac{s^2 C_n L_n + 1}{s^3 C_n L_n C_x + s(C_n + C_x)} \tag{6.8}$$

It has an imaginary zero at $\omega_z = 1/\sqrt{L_n C_n}$ and an imaginary pole at $\omega_p = \sqrt{(C_x + C_n)/L_n C_n C_x}$.

The zero is designed to be put at the image frequency while the pole is designed to be put at the desired RF frequency. The zero shunts away the image signal because the input impedance looking into the source of M2, which is $1/g_{m2}$, is designed to be much larger. On the contrary, at the desired RF frequency, Z_n is much larger than $1/g_{m2}$, conversion gain of the LNA remains unattenuated. In this way, the notch filter not only boosts image rejection but also diminishes the effect of the parasitic capacitance, C_x.

A negative gm cell with a current source is connected to the output of the LNA. It provides negative impedance across the LC tank, changes the quality factor of the LC tank and, ultimately, the conversion gain of the LNA. This helps to relax the linearity requirement of the receiver when the input power is large.

A two-bit switched capacitor array is also added at the output of the LNA to adjust the center frequency shift due to process variations. The simulation results are shown in Table 6.4.

Max voltage gain	S11	Noise figure	IIP3	Power consumption
26dB	-11.2dB	4.6dB	-13dBV	11mW

Table 6.4 Simulation result of the LNA

6.3.2 Mixer

A two-stage double-balanced down-conversion mixer is used. Its schematic is shown in Fig. 6.2. Each Gilbert cell has only 2 stacked transistors to minimize the voltage headroom required. Resistive load is used in the Gilbert cell for the sake of simplicity. The technique of current bleeding [42] is utilized to enhance the performance of the mixer under low-voltage supply.

A simplified mixer, as shown in Fig. 6.3, is used to illustrate the above technique. In order to study the limit of the circuit without current bleeding, the current source, I_1, is first ignored. The conversion gain of the mixer is proportional to the transconductance and, therefore, the bias current of M_1. However, increasing its bias current reduces the output DC voltage assuming other parameters remain unchanged. This reduces the voltage headroom of the LO and RF transistors, M_1-M_3, which is very critical for operation with 1V supply.

By using the technique of current bleeding, the bias current passing through the LO and RF transistors can be separated. A current source is used to inject current into the drain of the RF transistors, M_3. This can then increase the conversion gain of the mixer, without reducing the output DC voltage, the voltage headroom for M_1-M_3 and the linearity of the mixer under 1V supply.

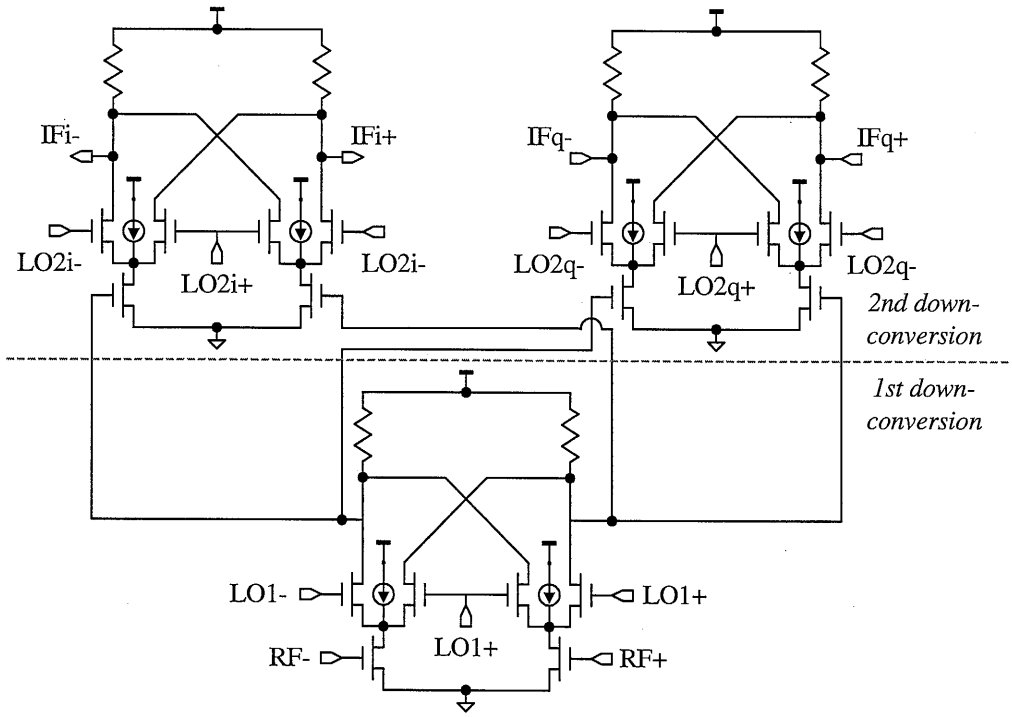


Fig. 6.2 Schematic of the down-conversion mixer

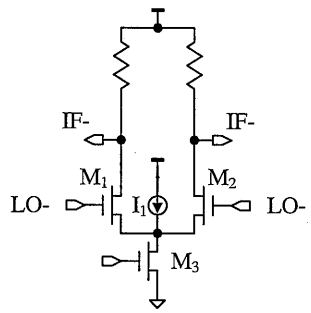


Fig. 6.3 Schematic of a simplified mixer

The RF inputs of the mixer are connected directly to the differential outputs of the LNA. LO1 is the first LO signal at 4.2GHz and LO2 is the second LO signal at 1.05GHz. Both of them are generated by the on-chip frequency synthesizer and amplified by buffers, which are used to sustain the signal strength through the long metal connections. A notch filter, similar to the one used in the LNA, is connected at the drains of the RF transistors in the first-stage mixer for image-rejection

enhancement. RC low pass filters are added at the quadrature outputs of the mixer to suppress the out-of-channel interferers. The simulation results are shown in Table 6.5.

Voltage gain	Noise figure	IIP3	Power consumption
-0.8dB	13dB	-10dBV	10mW

Table 6.5 Simulation result of the down-conversion mixer

6.3.3 Channel-Selection Filter

The fundamental objective of the channel-selection filter is to amplify the desired channel in the pass-band and provide sufficient attenuation for adjacent and alternate channels. Its other purpose is to filter out the DC offsets and the carrier feed through from the previous stage to prevent saturation of the following stages.

It is composed of five differential-pairs in cascade. Unbalanced Gm cell is used within the differential pair to improve the linearity. AC coupling is used in the first stage to filter out the DC offsets and carrier feedthrough. Its diagram and schematic is shown in Fig. 6.4.

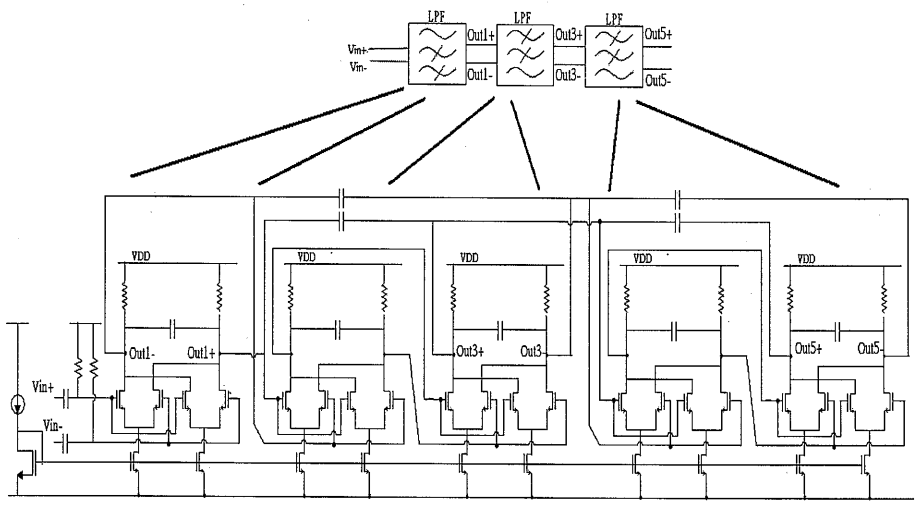


Fig. 6.4 Block diagram and schematic of the channel-selection filter

Instead of using simple first-order sections in cascade, local capacitive feedback is employed to achieve a fifth-order low-pass performance. The simplified half

circuit of the filter is shown in Fig. 6.5. By solving the nodal equation in the half circuit, its transfer function is given by,

$$H(s)=\frac{Vout(s)}{Vin(s)} \tag{6.9}$$
$$=\frac{GmR^3\left(Gm^2R+sC_{fb}+s^2C_{fb}RC\right)^2}{(1+sRC)\left[1+s\left(RC+RC_{fb}\right)\right]\left[1+s\left(3RC+3RC_{fb}-2R^3Gm^2C_{fb}\right)+s^2\left(3R^2C^2+6C_{fb}R^2C\right)+s^3\left(R^3C^3+3C_{fb}R^3C^2\right)\right]}$$

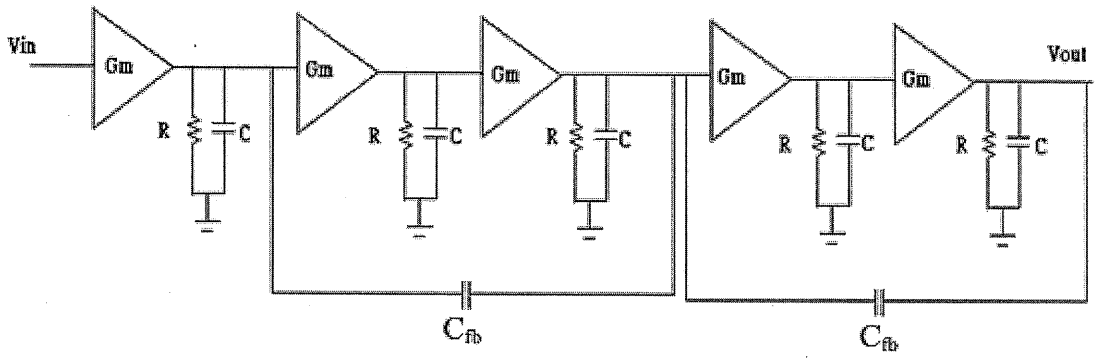


Fig. 6.5 Simplified half-circuit of the channel-selection filter

As shown in the above equation, two pairs of complex zeros are formed. The zeros create a notch and increase the attenuation at the frequency of interest. The frequency response of the above transfer function is shown in Fig. 6.6 together with the response of a simple cascade of 5 first-order sections for comparison. The attenuation with the local capacitive feedback is enhanced by at least 10dB.

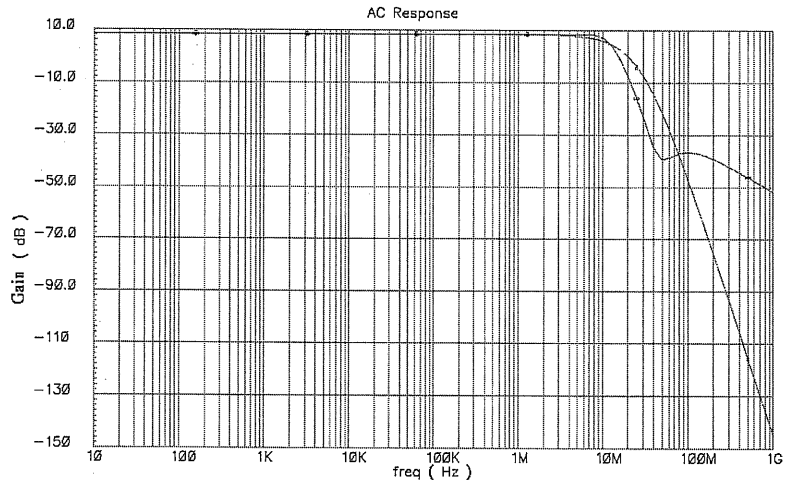


Fig. 6.6 Frequency response of the channel-selection filter

It should be noted that the local capacitive feedback also generates a pair of complex pole. Circuit parameters are carefully chosen to minimize peaking and to ensure the feedback is stable by preventing the formation of RHP pole. It is necessary to ensure that the following equation must be satisfied,

$$3RC + 3RC_{fb} > 2Gm^2R^3C_{fb} \tag{6.10}$$

The simulation results are shown in Table 6.6.

Voltage gain	Noise figure	IIP3	3dB frequencies	Stop-band attenuation	Power consumption
8.5dB	19.2dB	-12dBV	103.8kHz 10.9MHz	16.5dB@20MHz 41.8dB@40MHz	5mW

Table 6.6 Simulation result of the channel-selection filter

6.3.4 VGA

The block diagram of the VGA is shown in Fig. 6.7. It is composed of three identical variable gain cells together with its offset cancellation networks, a fixed gain cell and a received signal strength indicator (RSSI).

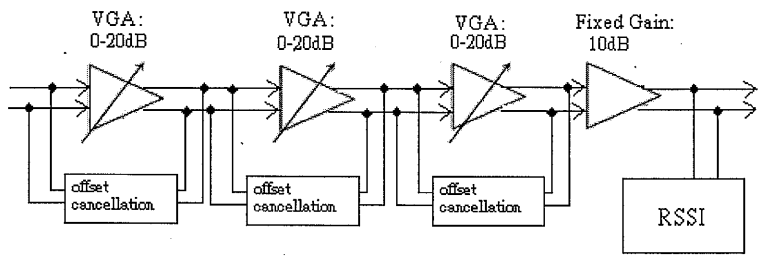


Fig. 6.7 Block diagram of the VGA

Conventional Gilbert cell, as shown in Fig. 6.8, cannot be used as the variable gain cell because it has 4 cascode transistors. The required voltage headroom is too large for low-supply operation. Output swing and linearity is, thus, limited.

Instead, a folded current steering gain cell [43] as shown in Fig. 6.9, is used as the variable gain cell. The bias currents, controlled by the voltage, *biasp*, and the gate

voltages of M_{5-6} are passed to the differential pairs M_{1-4} by the use of current mirrors. M_{5-6} are used to steer the differential current of M_{1-4} to the output according to the difference between the control voltage, V_c, and the reference voltage, V_r. If V_c is equal to V_r, the bias currents passing through M_{1-2} and M_{3-4} are the same. The transconductance of M_{1-4} is, therefore, equal. The ac drain currents from M_{1-4} cancel with each other at the output, resulting in zero voltage gain. If the difference between V_c and V_r is large, most of the bias current flows through either M_{1-2} or M_{3-4}. The ac drain currents are steered to the output without any cancellation, and the gain is, therefore, maximum.

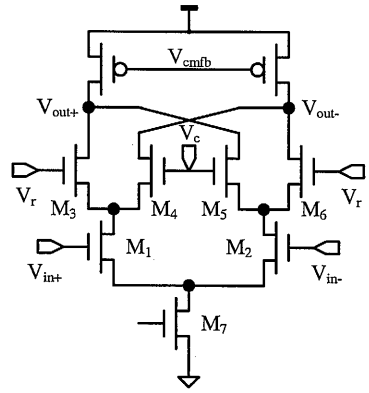


Fig. 6.8 Conventional Gilbert cell with current steering

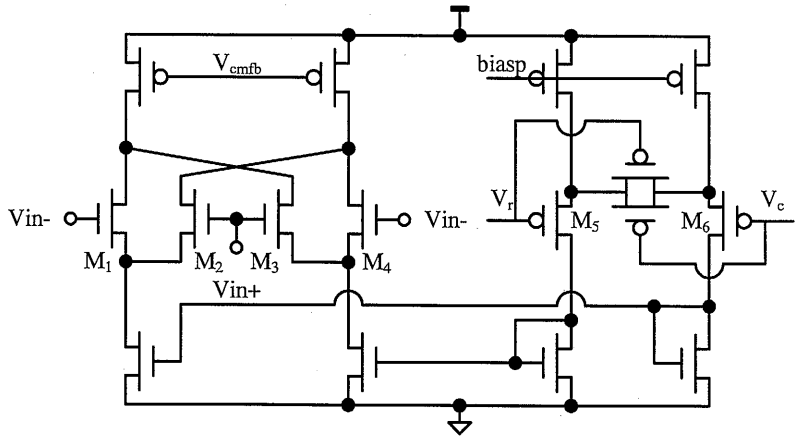


Fig. 6.9 Folded current steering gain cell

Since active-load is used in the gain cell, common-mode feedback, as shown in Fig. 6.10, is needed to stabilize the common-mode output voltage. The common-mode voltage level is sensed by $M_{16\text{-}17}$ and the error signal, V_{cmfb}, is fed back to the gate of the active-load in the variable gain cell.

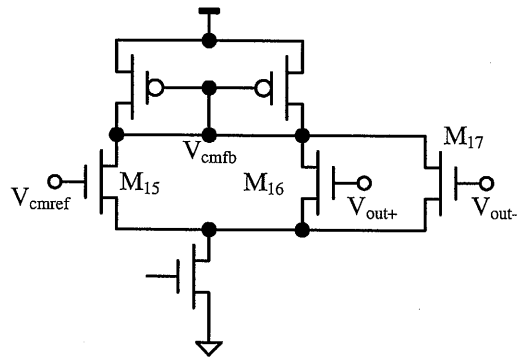


Fig. 6.10 Common-mode feedback amplifier

High pass filtering is necessary to remove the DC offset. Fig. 6.11 shows the offset compensation used in this VGA [44]. It used a low-pass filter as offset extractor and negative feedback to eliminate the offset voltage. The offset extractor and offset subtractor is realized, as shown in Fig. 6.12. The low pass RC section blocked the high frequency signal and extracted the DC offset voltage. Differential pair is used to convert the feedback voltage to current, which is used to subtract from the input current. When compared to ac coupling using resistor and capacitor, only one-fourth of the capacitance is required in this technique.

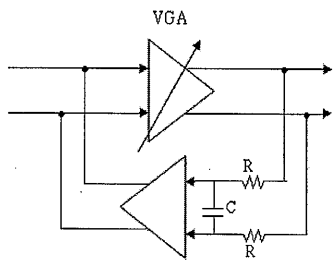


Fig. 6.11 Offset cancellation using negative feedback

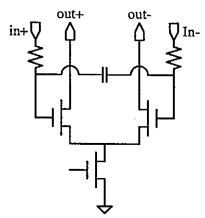


Fig. 6.12 Schematic of the offset extractor

In order to realize an automatic gain control with the baseband, a RSSI is needed to sense the output signal and produces a DC signal, indicating the output amplitude. This can be achieved by using a full-wave rectification circuit together with a low-pass filter [45]. The schematic of the RSSI used is shown in Fig. 6.13. It consists of switching devices $M_{r1\text{-}4}$, voltage to current differential pair M_{g1}, M_{g3} and current bias device M_{g2}, M_{g4}.

When the current flows in or out of the source of M_{r1} and M_{r2}, the devices will switch ON and OFF respectively and hence create a half-wave rectified current across M_{r2}. Full-wave rectification can be done by two identical paths in parallel which are driven by the differential input current from M_{g1} and M_{g3}. In order to filter out the high frequency components of the full-wave rectified current and convert it from current to voltage, the current is summed and filtered by a first order low-pass filter. In order to provide fine-tuning of the DC signal, the current from the current bias transistor M_{g2}, M_{g4} can be tuned and hence the zero crossing point between ON and OFF of the switching transistor can be varied.

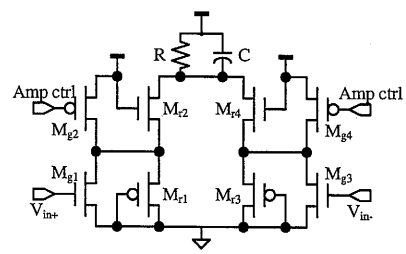


Fig. 6.13 Schematic of the RSSI

The simulation results are shown in Table 6.4.

Max voltage gain	Min noise figure	IIP3	3dB frequencies	Power consumption
70dB	16.6dB	-14.4dBV	91kHz, 24.9MHz	10mW

Table 6.7 Simulation result of the VGA

6.3.5 ADC

The ADC employs a 6-stage pipelined architecture to achieve 8-bit resolution while running at a sampling rate of 40Mbit/s. Its block diagram is shown in Fig. 6.14. A sample-and-hold circuit is employed to maintain good input bandwidth of up to 40MHz. It is then followed by 6 pipelined multiplying digital-to-analog converters with 1.5 bits per stage. Each of the MDAC subtracts appropriate reference voltages from the input signals and amplifies the resultant residue signal by two times.

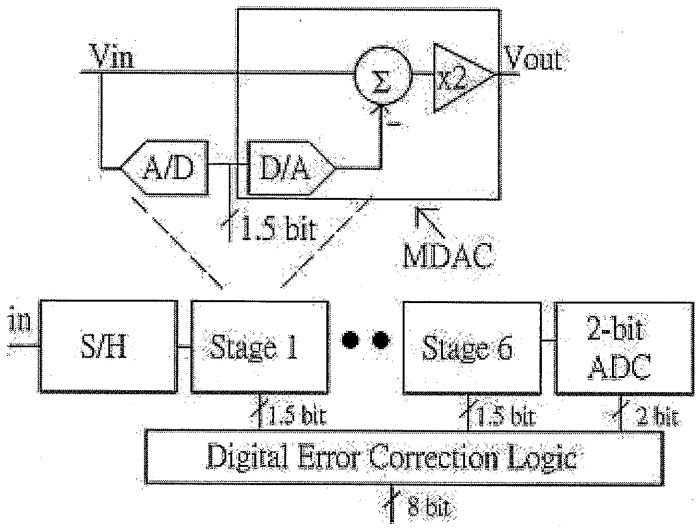


Fig. 6.14 Block diagram of the ADC

The schematic of a traditional switched op-amp (SO) MDAC is shown in Fig. 6.15. At supply voltage as low as 1V, the series switches attached to the output of the op-amp cannot be turned on properly. Thus, these problematic switches are replaced by switched op-amps whose outputs are reset to a desirable voltage, e.g., 0V, when the op-amp is inactive.

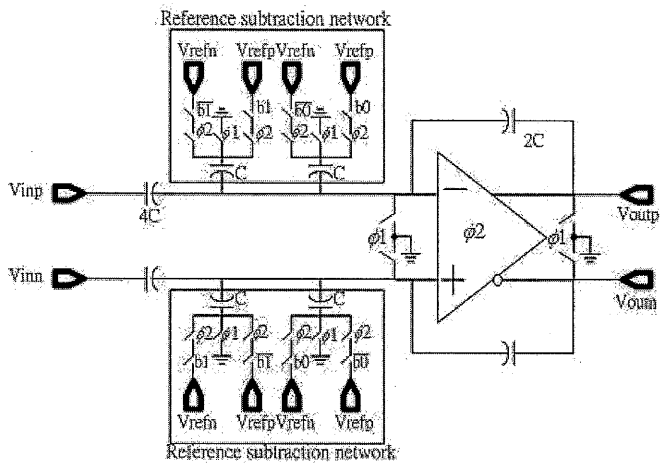


Fig. 6.15 Schematic of a traditional SO MDAC

However, in such SO MDAC, the sampling capacitor, labeled as *4C* in Fig. 6.15, is always connected to the output of the previous stage. This reduces the feedback factor of the SO MDAC and slows down its speed. In order to correct these problems, a novel loading-free MDAC proposed by *Vincent Cheung* and *Patrick Wu* in the Analog Electronics Research Group in the Hong Kong University of Hong Kong, as shown in Fig. 6.16, is used.

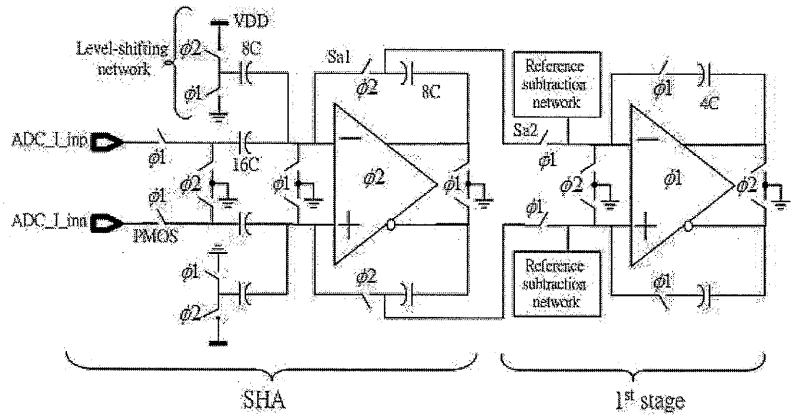


Fig. 6.16 Schematic of the sample-and-hold circuit and the proposed MDAC

Compared to the traditional MDAC as shown in Fig. 6.15, the sampling capacitors in the proposed loading-free MDAC are removed to help reduce the loading capacitors and enhance the speed of the previous stage. The removal of the sampling capacitors is possible based on the fact that the feedback capacitors of the

previous stage, labeled as *8C*, store the charge corresponding to the output voltage when the op-amp finishes settling in Φ2. Instead of resetting this charge in the next Φ1, the charge is transferred to the next stage's feedback capacitors, labeled as *4C*. In order to achieve this "loading free" architecture, two additional switches, *Sa1* and *Sa2*, are added.

It should be noted that this loading-free architecture cannot be used throughout the whole pipeline since the feedback capacitor needs to be scaled up by two times along the pipeline to achieve the "x2" function in MDAC. This would cause the capacitor spread to be too large. Therefore, the proposed architecture is applied only to the critical stages, namely the first and the second stages right after the sample-and-hold circuit. The remaining stages use the traditional SO MDAC.

The switched-op-amp is shared between the two quadrature channels using time-multiplexing. Area can, thus, be saved, and better symmetry can be obtained between the two channels.

The full-scale differential input for the ADC spans from -500mV to +500mV. Therefore, the output DC level of the VGA is set to be 0.75V, with single-ended signal swing of 0.25V. In order to give full-scale input signals to the subsequent stage, the sample-and-hold stage is required to multiply the sampled signal amplitude from the VGA by two.

The simulated SFDR of the ADC is 48.5dB

6.4 Circuit description of the building blocks in the transmitter

6.4.1 DAC

An 8-bit current-steering, segmented DAC is used. It is a mixture of the thermometer and binary-weighted topologies. The segmented architecture is a

compromise between the two topologies. It helps to minimize the distortion due to the large glitch energy in a pure binary-weighted topology. It also helps to reduce the complexity of the decoding logic and chip area in a pure thermometer topology.

The block diagram of the DAC is shown in Fig. 6.17. The 5 MSBs are implemented using the thermometer architecture while the 3 LSBs are implemented with the binary-weighted architecture. Two-dimensional centroid switching sequence, similar to the one described in [46], is implemented in the thermometer section. By simultaneously selecting a symmetrically located current source in each of the four quadrants of the matrix, the systematic error is minimized. The 5 MSBs are decoded into 32-bit thermometer control signals. A two-stage, row-column decoding logic is implemented for them. It only requires NAND and NOR gates with three or two inputs.

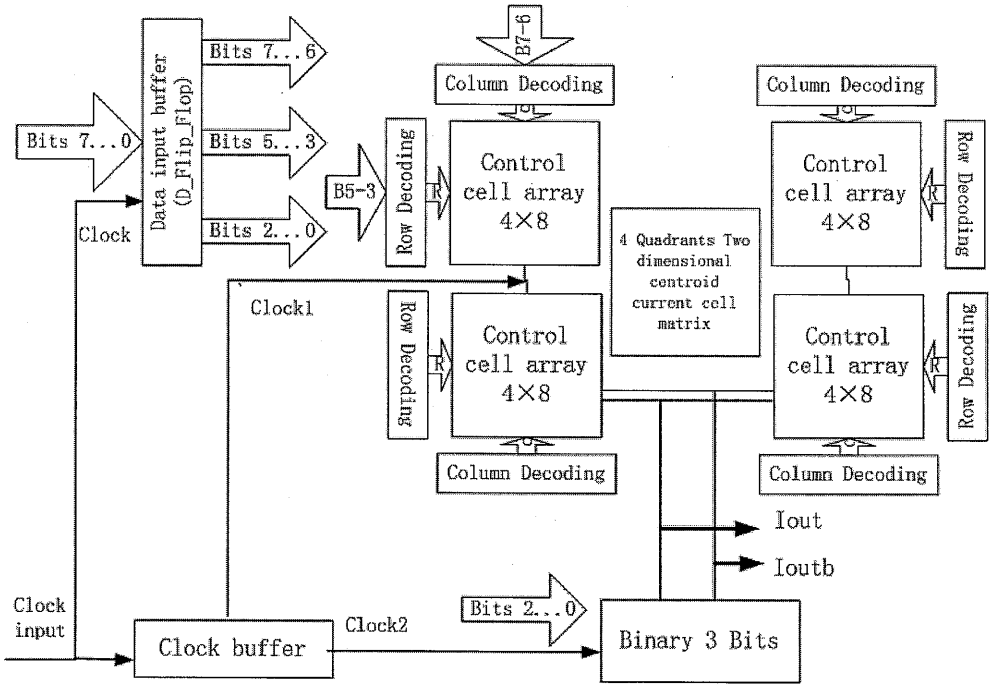


Fig. 6.17 Block diagram of the DAC

Fig. 6.18 shows the schematic of the current cell. It is composed of the cascode current mirror transistors, $M_{1\text{-}2}$, switch transistors, $M_{3\text{-}4}$, and dummy transistors

M5-6. Matching of the current sources is very critical to the performance of the DAC. By using a normal distributed model for random mismatch, the total charge current is selected to be 1.5mA for the best matching. The width and length of the unit transistor, M_1, is chosen to be 2.5 um and 4 um respectively.

The impedance at the output nodes is changed when different numbers of current sources are switched to the outputs. This is unfavorable to the linearity of the DAC. Thus, cascode current mirrors are employed to increase the output impedance.

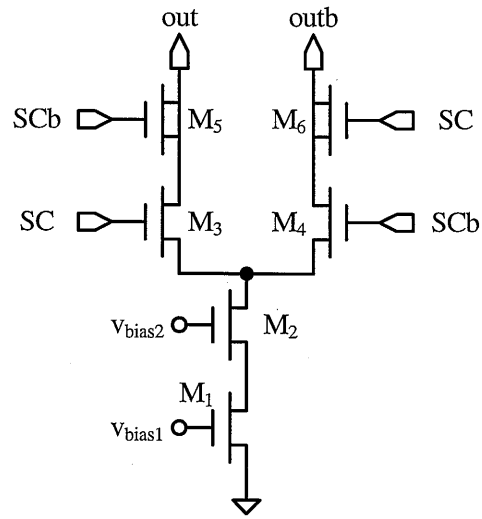


Fig. 6.18 Schematic of the current cell

The control signals driving the switching transistors are buffered by latches as shown in Fig. 6.19. In the latch, the positive feedback loop, consisting of $M_{1\text{-}4}$, helps to reduce the switching time. In order to prevent coupling, the buffers at the outputs of the feedback loop are connected to a supply voltage separated from that for the control output signals.

Coupling of the switching control signals to the output lines may also occur because of the parasitic capacitance of the switching transistors. It can create undesirable glitches to the output. In order to remedy this problem, two dummy

transistors, $M_{5\text{-}6}$ are connected in series with the switching transistors. They are also driven by complementary control signals. In this way, undesirable feedthrough and charge injection can be minimized.

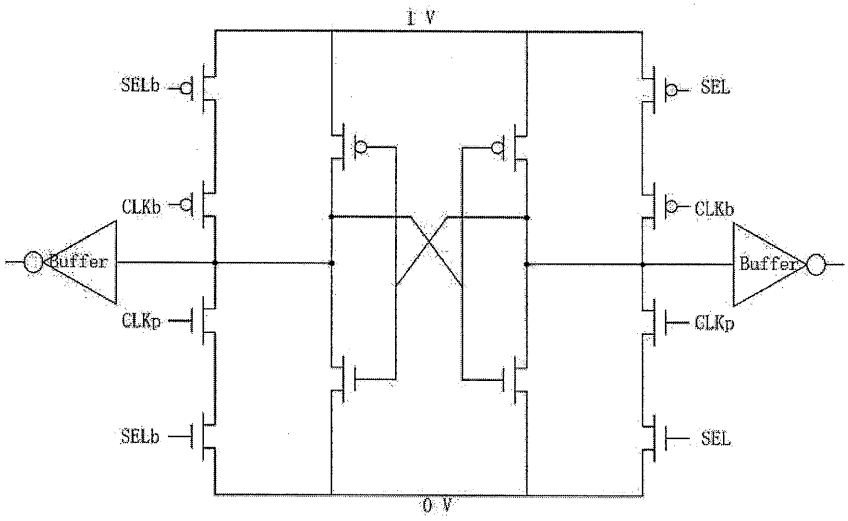


Fig. 6.19 Schematic of the latch driving the switching transistors

The simulation results are shown in Table 6.4.

DNL/INL	SFDR	Power consumption
0.04/0.025	64dB	1.9mW

Table 6.8 Simulation result of the DAC

6.4.2 Filter

A third-order band-pass filter is connected at the output of the DAC. Its schematic is shown in Fig. 6.20. It consists of 3 identical low-pass passive RC filters and employs a DC-decoupling input branch for generating a specific DC bias for the up-mixer.

Since the filter only consists of passive devices, it achieves excellent linearity and zero power consumption. In order to minimize the process variation of lump elements, the resistor as wide as 2μm and differentially inter-digitized capacitors are used.

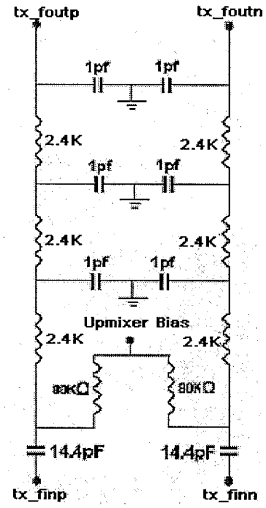


Fig. 6.20 Schematic of the transmission filter

The simulation results are shown in Table 6.9.

Voltage gain	3dB frequencies	Stop-band attenuation
-2.9dB	101 KHz 12.5 MHz	-11.65dB@30MHz -14.35dB@40MHz

Table 6.9 Simulation result of the transmission filter

6.4.3 Up-conversion mixer

A single sideband mixer is used to implement the up-conversion mixer. The single sideband mixer is composed of three double sideband mixers. Fig. 6.21 shows the block diagram and the graphical analysis of the mixer. The quadrature baseband inputs are first up-converted by the 1GHz LO1 in the first-stage mixer. Its output signals are then combined and further up-converted by the 4GHz LO2 in the second-stage mixer.

In Fig. 6.21, the complex numbers on top of the signal spectra denotes the phase relations of the spectra at different internal points of the mixer. Quadrature baseband signals from the output of the DAC are applied to the corresponding quadrature paths at the input of the mixer. The input spectrum convolves with the quadrature LO signals at the first stage of the mixer and generates the spectra at points A and B. Because the +j input spectrum convolves with –j/2 in the positive frequency, the

positive frequency part of the spectrum at point B is in-phase with that at point A. Similarly, the negative frequency part of the spectrum at point B is exactly out-of-phase with that at point A. By adding these spectra together, only the upper sideband remains in the signal path.

The second stage of the mixer is also a double sideband mixer. It generates the undesired lower sideband again. Yet, it is a relatively weak signal because it is around 2GHz away from the desired sideband. The lower sideband is, thus, attenuated by the LC tank at the output of the second-stage mixer.

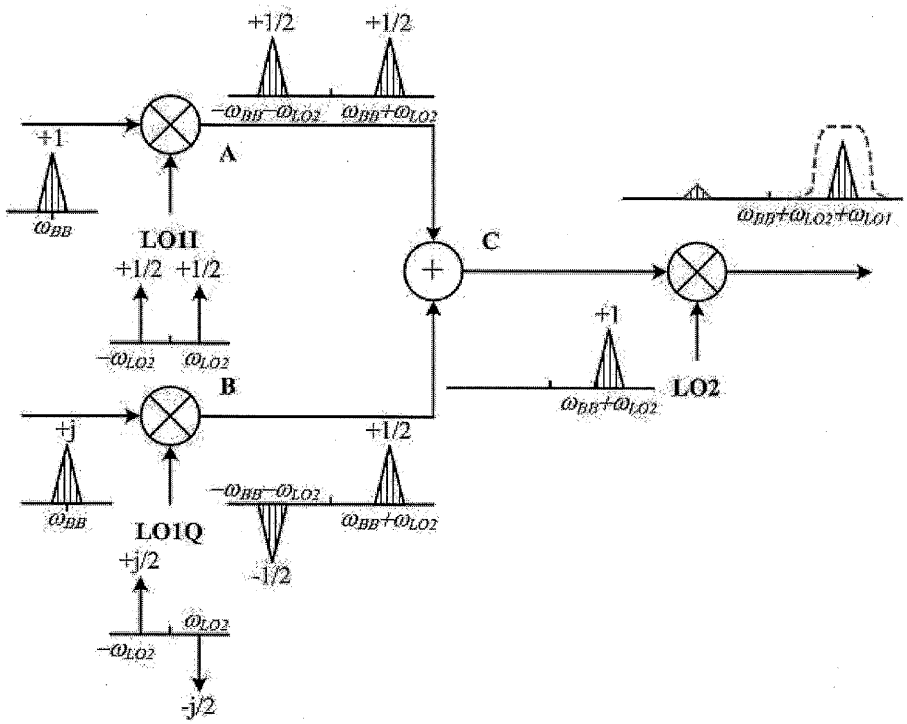


Fig. 6.21 Block diagram of the single-sideband up-conversion mixer

The schematic of the up-conversion mixer is shown in Fig. 6.22. The first-stage mixer is implemented using a modified, doubly-balanced Gilbert multiplier. In conventional Gilbert multiplier, differential RF inputs are applied to the common-source MOS at the bottom of the LO switching transistors. In contrast to the conventional Gilbert multiplier, the baseband signals are applied to the gate

inputs of the MOS, configured as a source follower [47], instead of the gate of the common-source MOS at the bottom of the LO switching transistors in conventional multiplier. In such configuration, the drain of the input NMOS is connected to the supply voltage. Its drain-source voltage is no longer limited by voltage drop due to the cascode transistors on the top. Since the source of the input NMOS is connected to a current source, the bulk of the NMOS is connected directly to its source to minimize the threshold voltage. This can be achieved by putting the NMOS in deep nwell, which is available in the process. The input voltage swing and, therefore, the linearity can be maximized.

The second-stage mixer is a simple Gilbert multiplier with inductive load. SCA is added at the output of the mixer to compensate for the shift in center frequency due to process variations. Similarly, the technique of current bleeding used in the down-conversion mixer is also utilized in the up-conversion mixer. Therefore, as mentioned previously, the conversion gain, noise figure and linearity of the second-stage mixer can be enhanced.

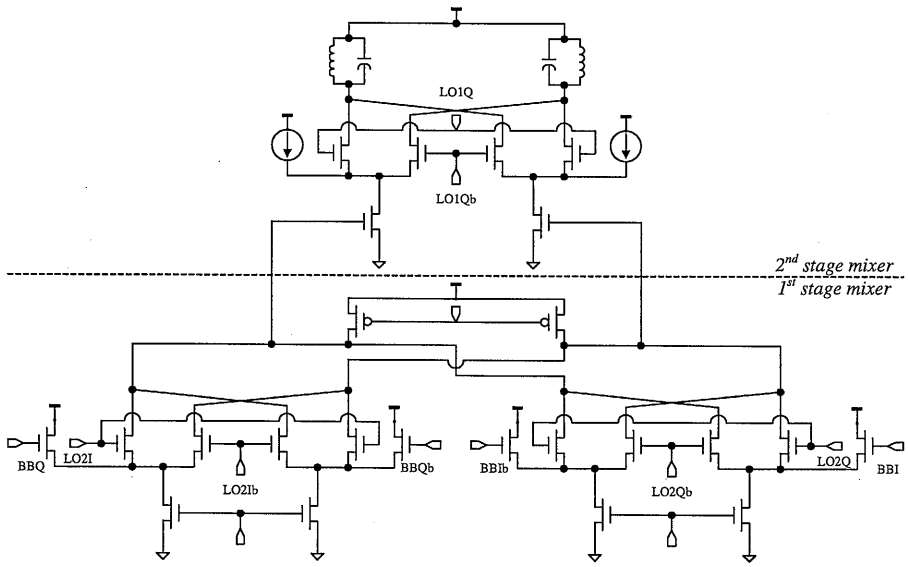


Fig. 6.22 Schematic of the up-conversion mixer

The simulation results are shown in Table 6.10.

Voltage gain	OIP3	Power consumption
2.2dB	-18dBV	14mW

Table 6.10 Simulation result of the up-conversion mixer

6.4.4 PA

The on-chip PA is used as a pre-amplifying stage for the external PA. Its schematic is shown in Fig. 6.23. Because of OFDM, high peak-to-average ratio is required in the system. This calls for a highly linear PA for transmitting the OFDM signal. Hence, a two-stage class-A topology is selected for the PA. The common-source configuration is used since it provides the highest efficiency when compared to its common-gate and common-drain candidates. One drawback of the class A amplifier is its poor efficiency which is a result of its 360° conduction angle. Its efficiency can be expressed as,

$$\eta = \frac{P_{out}}{P_{supply}} \leq \frac{V_{DD}^{\ 2} / R_L}{V_{DD}^{\ 2} / 2R_L} = 50\% \qquad (6.11)$$

Thus, the maximum achievable efficiency is 50%. The actual efficiency drops when non-idealities are taken into account. Yet, the target output power of the on-chip PA is 0dBm, which is equivalent to 1mW. Even if the efficiency drops to 10%, the power consumption of the PA is around 10mW. This power consumption is still within the budget.

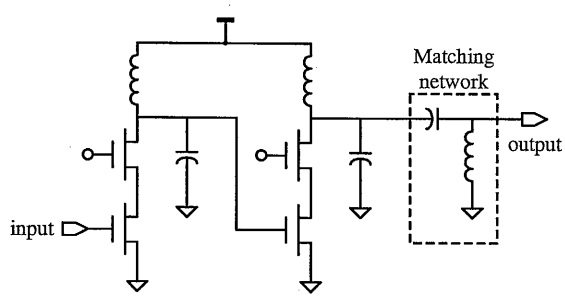


Fig. 6.23 Schematic of the PA

SCA is connected at the output of each stage to compensate for the shift in center frequency due to process variations. A matching network is connected to the output of the PA externally. It helps to transform the output impedance of the PA to 50Ω. This is necessary for maximum power transfer when the external PA is connected together with the on-chip transmitter.

Stability is a critical issue for a PA. The necessary and sufficient conditions for unconditional stability [48] can be summarized mathematically as,

$$\begin{cases} K = \dfrac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} > 1 \\ |\Delta| = |S_{11}S_{22}-S_{12}S_{21}| < 1 \end{cases} \tag{6.12}$$

It can be noted that the smaller the value of S_{12}, the easier the above conditions can be fulfilled. One simple way to reduce its value is to add a cascode transistor between the input device and the load in each stage of the PA. The reverse isolation and, hence, the stability of the PA, can be greatly enhanced. The simulation results are shown in Table 6.4.

Power gain	Output P_{1dB}	OIP3	Power consumption
10dB	3dBm	0dBV	5.6mW

Table 6.11 Simulation result of the PA

Chapter 7 Experimental results of the prototype

7.1 Floorplan and layout of the prototype

The floorplan of the transceiver is shown in Fig. 7.1. The layout of the prototype is arranged in a rectangular shape in order to increase the number of peripheral pads for more flexible testing purpose. The longer the layout is, the longer the perimeter and the more peripheral pads the prototype allows.

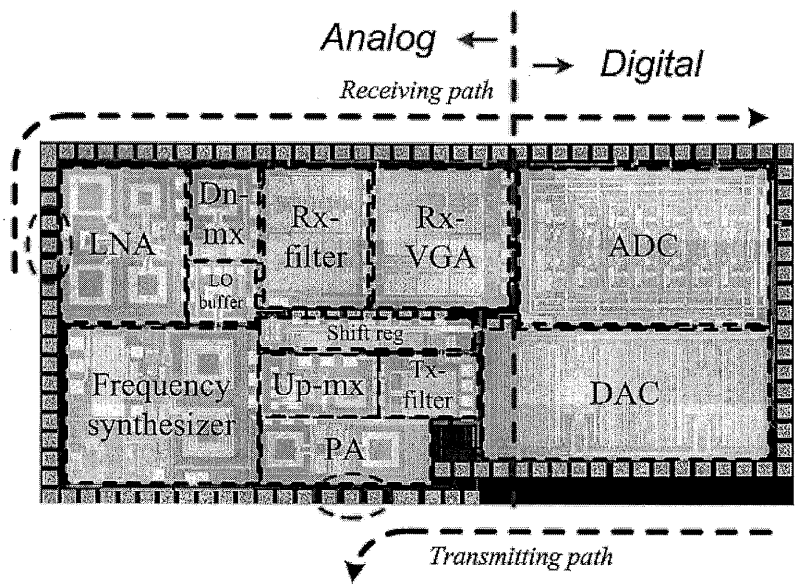


Fig. 7.1 Floorplan of the transceiver

In the floorplan, the analog part is put on the left and digital part is put on the right. The partition is indicated by a vertical dash line as shown in Fig. 7.1. The purpose is to maximize the distance between the analog and digital signals. In additional to the guard rings encircling each building block, many substrate contacts are put in between the analog and digital sections to minimize noise coupling from the digital building blocks to the noise sensitive analog circuits through the substrate. Supply and ground for analog and digital circuits are carefully separated in order to reduce noise coupling through the supply or ground.

Another partitioning is done according to the signal path in the transceiver. The receiving path is put on the top of the floorplan. The receiving signal runs from the LNA on the left to ADC on the right, with all the building blocks in the receiver lining up in a straight line, one after another. This arrangement allows the shortest metal connection between the building blocks. The input signal is split and transmit in quadrature paths after the second mixing with the LO signals. Special caution is taken to ensure the symmetry of the quadrature paths so as to minimize the layout mismatches.

The input to the LNA is put on the left top corner, which locates farthest from the digital parts. This is critical because the LNA input signal is small and noise sensitive. Any noise coupling can affect the SNR and sensitivity of the whole receiver significantly.

The transmitting path is put on the bottom. The area occupied by the transmitter is much smaller than that by the receiver. Its signal path no longer runs from one side to the other. The transmitting signal starts from the DAC on the left edge and ends at the PA output in the center of the bottom edge. The shortest metal connection between building blocks can be facilitated. In addition, this allows the frequency synthesizer to be put on the left bottom corner, just right beside the up-conversion mixer.

As operating frequency increases, the transmission-line effect in metal connection gets more and more significant. At a frequency of 5GHz, the transmission-line effect is no longer negligible. Thus, the metal connection between the up-conversion mixer and the PA has to be as short as possible.

This is particular critical to the LO buffer in the frequency synthesizer because it drives both the down-conversion and up-conversion mixers. The loading of the

mixers, as well as the transmission-line effect can significantly attenuate the LO signals. Hence, the routing metal among the LO buffer and the mixers is shortened as much as it can. An optimal location for the LO buffer is below the down-conversion mixer and the left top corner of the up-conversion mixer.

The proposed WLAN transceiver integrating all the building blocks is fabricated in a 0.18-μm CMOS process (VTn = 0.52 V, VTp = - 0.54 V) with 6 metal layers. Fig. 7.2 shows the chip photo of the transceiver, which occupies only 12.5mm^2.

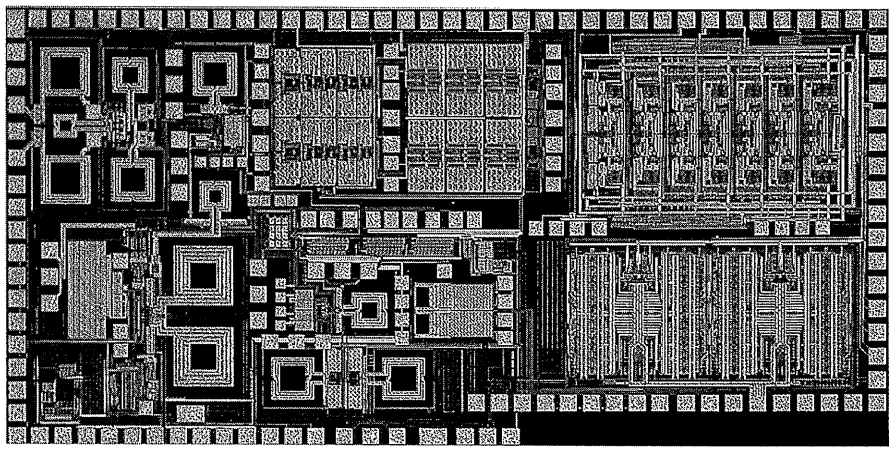


Fig. 7.2 Chip photo of the transceiver

In order to allow for on-wafer measurement, SGS probes are applied on top of the differential testing pads to inject or receive RF input or output signals. Pads with a minimum size of 50μm×50μm are used for the probes. In order to minimize the parasitic capacitance, all these pads are only composed of two metal layers, metal 5 and metal 6, which are the farthest from the substrate. Metal 5 is used to connect the probes to the ground. It also acts as a ground shielding to reduce the noise coupling from the substrate to the input or output signals.

Other pads are used for the connection of DC bias. Since DC bias is applied through bondwires, pads with a size of 90μm×90μm are used. This is to ensure that

the bondwires can be bonded onto the pads. All the pads for DC bias consists of all the 6 metal layers.

7.2 Measurement setup

To measure the proposed transceiver, its die is glued using silver paint onto a double-layer PCB directly, as shown in Fig. 7.3. The die is also glued in a CerQuad package with 100 pins, as shown in Fig. 7.4. The DC biases are wire bonded onto the PCB. A larger amount of SMD capacitors are soldered to the pins for power supply and DC biases to short any interference or noise. A large amount of vias are also used to connect the ground plane on both sides of the PCB. High-frequency input and output signals are then applied using microwave differential probes, as shown in Fig. 7.5.

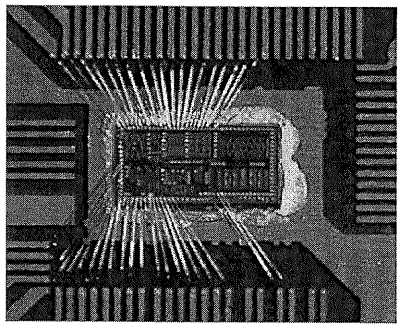


Fig. 7.3 Die of the proposed transceiver on a PCB

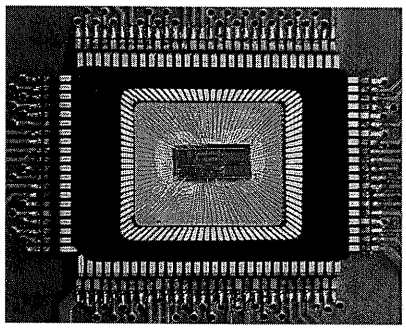


Fig. 7.4 Die of the proposed transceiver in a CerQuad package

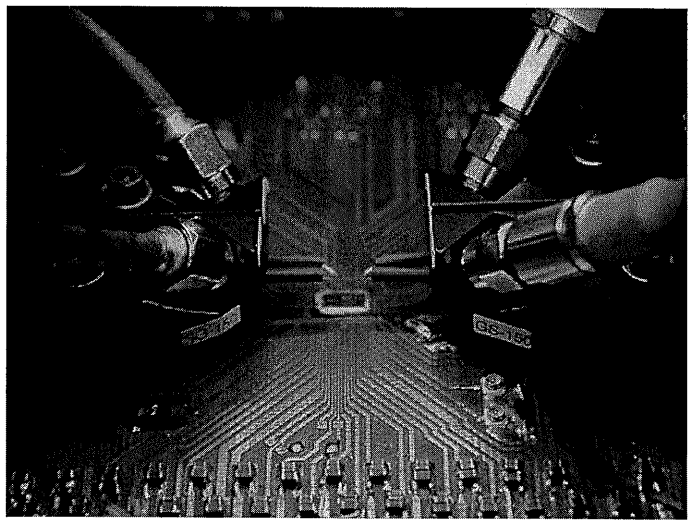


Fig. 7.5 Microwave differential probes, transceiver die and the evaluation board

7.2.1 Testing setup for the receiver

The general setup for the measurement of the receiver is shown in Fig. 7.6. DC biases are applied externally through bondwires. Input signals are generated from the signal generator, *Agilent E4438C*, and applied into the receiver utilizing differential microwave probes. The output of each stage of the receiver is buffered by a 50Ω open-drain buffer. The differential output signals from the buffer are then obtained by differential microwave probes stage by stage. They are represented by the probes in bold in Fig. 7.6. The differential probes are connected to a hybrid combiner and then connected to network analyzer, spectrum analyzer and oscilloscope for different measurement respectively.

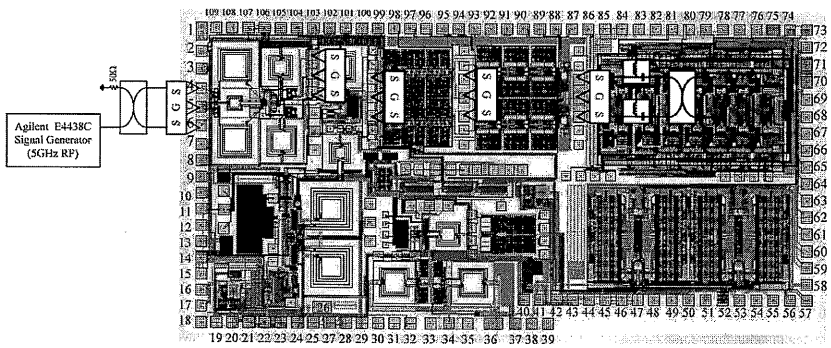


Fig. 7.6 Setup for the measurement of the receiver

The measurement is started by testing the input matching of the receiver. Before placing the differential microwave probe at the input pads of the receiver, it is calibrated using a calibration substrate to move the reference plane for measurement to the probe tips and compensate for the losses of cables, probes and connectors. After the calibration, the differential microwave probe is then connected to Port 1 of the network analyzer. S_{11} is obtained and analyzed.

This is followed by the measurement of the frequency response and conversion gain. This is done by getting the signal from the 50Ω open-drain buffer from each stage into the spectrum analyzer. Different input power levels are applied. Voltage gain of the receiver is adjusted continuously by the control voltage, with the output fixed at the same power level.

Similarly, linearity is measured with two sinusoidal interferers being input into the receiver instead of one single tone. Since out-of-channel IIP3 is tested, the two tones are one channel bandwidth, which is 20MHZ, apart from each other. Intermodulation between the two interferers should be carefully removed before being injected into the input of the receiver. This can be achieved by using the *IMD suppression* available in the *multi-tone enhancement signal studio* to correct the distortion.

Noise figure is then measured by using the spectrum analyzer. Noise floor is observed when the input of the receiver is terminated with 50Ω impedance. The attenuation of the cables, hybrid combiner as well as the differential microwave probes can significantly increase the input noise power density. It is, therefore, critical to calibrate out these losses when measuring the noise figure of the receiver.

7.2.2 Testing setup for the transmitter

The general setup for the measurement of the transmitter is shown in Fig. 7.7. DC biases are applied externally through bondwires. Differential quadrature input signals are generated from the vector signal generator, *Agilent E4438C*. Because the input signals are within 10MHz, at which attenuation and matching requirement is much relaxed, they are applied at the input of the filter of the transmitter through bondwires. Differential microwave probes are then used to obtain the RF output signals from the 50Ω open-drain buffer of the up-conversion mixer. The outputs of the PA are connected to the matching networks on the PCB using bondwires. Because the output bandwidth is 20MHZ, simple LC matching networks are used. The output signals at the matching networks are then combined by a hybrid coupler and connected to the input of an external PA.

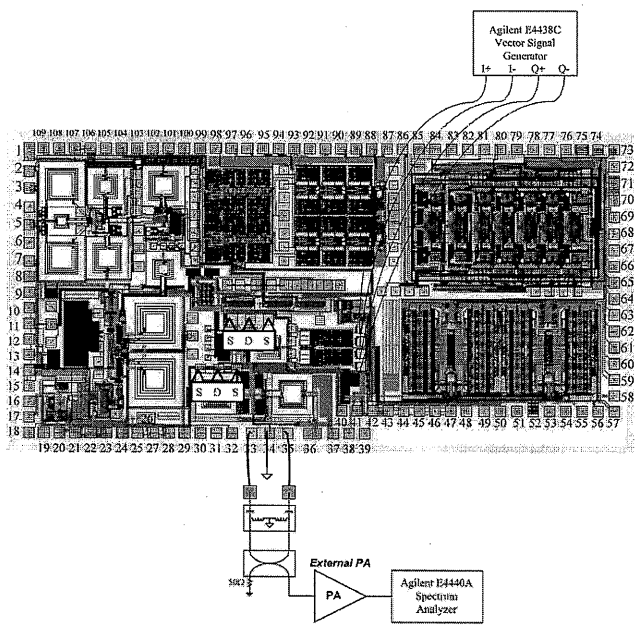


Fig. 7.7 Setup for the measurement of the transmitter

The output signals at the up-conversion mixer, on-chip PA and external PA are connected, one by one, to the spectrum analyzer for the measurement of conversion gain and output-referred 1-dB compression point.

System measurement is done at the outputs of the on-chip PA and external PA respectively using the vector signal analyzer, *Agilent 89611A*. Differential quadrature IEEE 802.11a modulated signals are created using the *Signal Studio for IEEE 802.11a* software. The modulated signals are injected into the filter using the *Agilent E4438C*. Modulated output spectrum, constellation diagram and EVM are then available using the vector signal analyzer using the WLAN modulation analysis.

7.3 Measurement results of the receiver

7.3.1 Input matching

The input matching, represented as S_{11}, is shown in Fig. 7.8. As shown in the figure, the best input matching is obtained at around 5.5GHz. It is around 300MHz higher than the center frequency of the desired frequency range. This frequency shift is due to process variations in the input transistor and gate and source inductors of the LNA. Within the desired frequency range, the value of S_{11} changes from -13.4dB at 5.15GHz to -21.3dB at 5.35GHz. This is smaller than the typical value for good input matching, which is around -10dB.

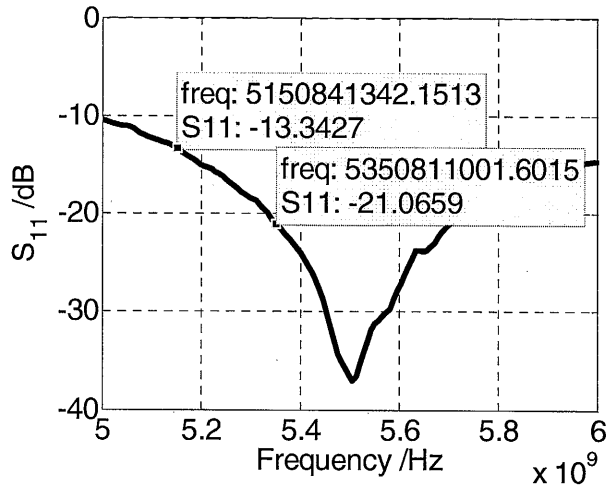


Fig. 7.8 Input matching of the receiver

Assuming that the reverse transmission from the output of the VGA to the input of the LNA is very large, the input reflection coefficient of the receiver is defined as,

$$\Gamma_{in} = S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{7.1}$$

where Z_{in} is the input impedance looking into the LNA and Z_0 is the characteristic impedance

The characteristic impedance in this system is 50Ω. The corresponding input impedance of the receiver is 50.7Ω at 5.15GHz to 54.8Ω at 5.35GHz. The variation is around 7.7%.

7.3.2 Conversion gain

Conversion gain of the receiver is measured by injecting an input with a fixed power level. The frequency of the LO and RF signals are changed to generate an IF with a fixed frequency. The conversion gain is then obtained by subtracting the output power at the VGA from the RF input power. The measured conversion gain of the receiver is shown in Fig. 7.9.

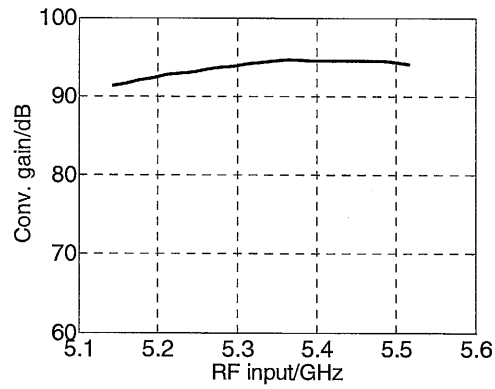


Fig. 7.9 Conversion gain of the receiver in the IEEE 802.11a lower and middle bands

The maximum voltage gain achieved is 94.5dB. This is 8.5dB larger than the specified voltage gain, which is 86dB. Table 7.1 shows a comparison about the

breakdown of the specified and measured voltage gain for each building block in the receiver. As shown in the table, the 8.5dB increase in the maximum voltage gain is the result of the increased voltage gain in the LNA and the VGA.

Building block	LNA	Down-mixer	Filter	VGA	Total
Specified voltage gain /dB	21	0	10	55	86
Measured voltage gain /dB	25.2	-1.1	10.7	59.7	94.5

Table 7.1 Breakdown of voltage gain for each stage in the receiver

The center frequency is located at 5.36GHz. The center frequency is shifted up by around 100MHz from the desired center frequency, which is specified to be 5.25GHz. The actual process variations in the transistors and inductors used in the LNA are larger than the expected ones. Therefore, although all of the SCAs connected at the outputs of the LNA are already turned on to compensate for the variations, the center frequency is still 100MHz larger.

The 3-dB bandwidth for the RF input is measured to be 400MHz. From 5.15GHz to 5.35GHZ, the voltage gain changes from 91.5dB to 94.5dB. The voltage gain at 5.15GHz can still meet the specification with a 5.5dB margin. In case flat gain is required across the whole frequency band, the voltage gain of the VGA can be tuned continuously by a DC bias.

Fig. 7.10 shows the transient maximum VGA output signal when the RF input is down-converted. The signal has a voltage of $0.47V_{pp}$ at 1MHz. The DC output is 0.74V. By varying the gain control voltage of the VGA, the output voltage is adjusted. The measurement result is shown in Fig. 7.11. The range of the voltage gain can be adjusted from 31dB to 94.5dB by varying the gain control voltage in the VGA alone. When the control voltage is increased, the voltage gain also increases non-linearly and gets saturated when the control voltage is larger than 0.5V. When the receiver is integrated with the baseband processor, the voltage gain of the

receiver can be controlled by using a look-up table (LUT) for mapping the voltage gain and the control voltage. The digital output of the LUT can then be converted into the analog domain by using a DAC.

To achieve lower voltage gain, the negative gm cell in the LNA can be turned off and the voltage gain of the filter can also be adjusted. This can reduce the total gain to as low as 14dB. This is 20dB lower than the specified minimum voltage gain, which is 34dB. Hence, the range of the voltage gain can cover the specification with a great margin.

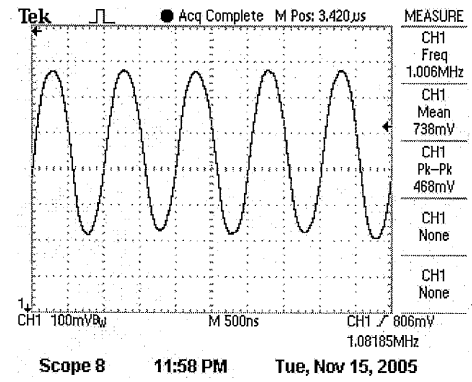


Fig. 7.10 Transient waveform at the output of VGA

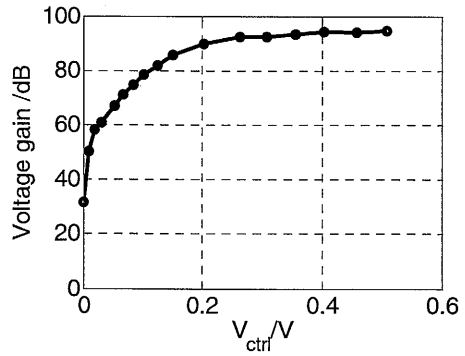


Fig. 7.11 Output power of the receiver as a function of V_{ctrl}

7.3.3 Frequency response

The frequency response at the output of the receiver is then measured. It is determined by the low-pass characteristic at the output of the mixer and the

band-pass characteristic of the channel-selection filter. It is not affected by the LNA because it has a signal bandwidth much larger than the channel bandwidth. The measurement is done by injecting LO signals fixed at a particular frequency and RF signal with varying frequency. The voltage gain at the output of the VGA against frequency offset of the IF signal can be measured. The measurement result is shown in Fig. 7.12.

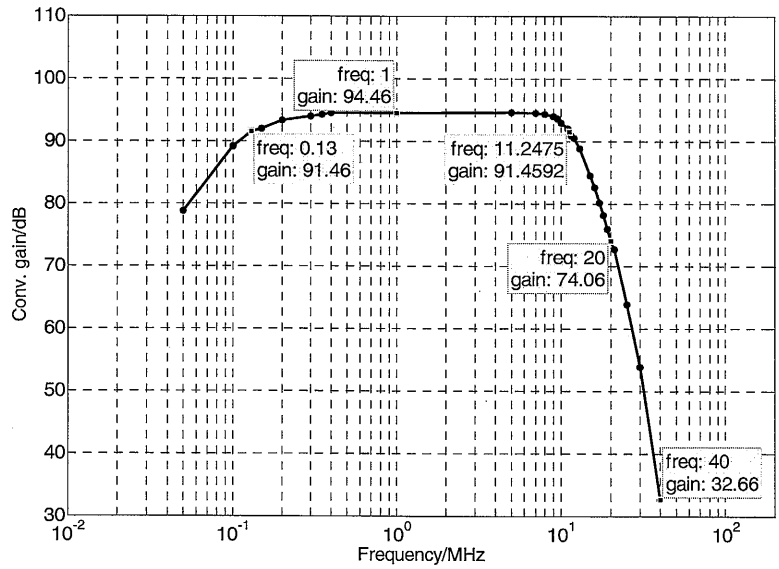


Fig. 7.12 Frequency response of the receiver as a function of IF output

As shown in the figure, the lower and upper 3-dB frequencies are 130kHz and 11.2MHz respectively. The attenuation at 20MHZ and 40MHz is 20.4dB and 61.8dB respectively. The band-pass characteristic can help to suppress the DC offset without affecting the information in the channel and achieve the specified attenuation requirements which are 15dB and 30dB at 20MHz and 40MHz respectively.

The frequency response of the VGA is also band-pass. It is measured by a network analyzer and its measurement result is shown in Fig. 7.13. The lower and upper 3-dB frequencies are 72.2kHz and 30.5MHz. Because the 3-dB bandwidth of the VGA is much wider than that of the filter, the frequency response of the VGA

does not limit the bandwidth of the receiver but only helps to increase the attenuation outside the desired channel bandwidth.

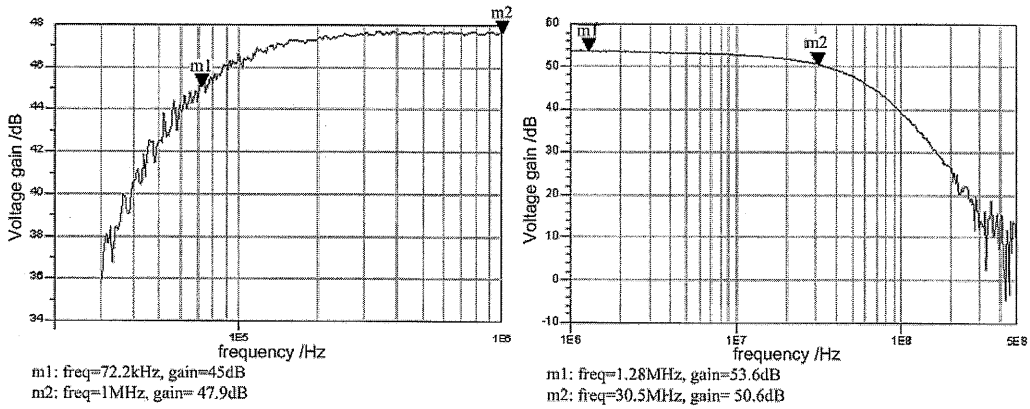


Fig. 7.13 Frequency response of the VGA

7.3.4 Linearity

7.3.4.1 IIP3

Two out-of-channel interferers are generated by the *multi-tone enhancement signal studio* available in the signal generator. It is split into differential signals using a hybrid coupler and applied to the input of the receiver. The frequencies of the two interferers are 5.275MHz and 5.295MHz respectively. Because the interferers are attenuated by the channel-selection filter when they reach the output of the VGA, the relation between the input and output power of the in-band, in-channel fundamental tone is found in another measurement but using the same setup. Instead of applying two interferers, a single sinusoidal tone at 5.255GHz is input into the receiver. The RF input is then down-converted to 5MHz, which is the same as that of the intermodulation products. It is then compared with the intermodulation products. By extrapolation, the IIP3 can be found.

IIP3 when the receiver is set to different voltage gains, by adjusting the gain control bias of the VGA, are shown on Fig. 7.14 altogether. The output power of the fundamental tones, in circle, and the intermodulation products, in square, are plotted

against the corresponding input power, with a slope of one and three, respectively. The four sets of curves are extrapolated to find the IIP3. The IIP3, indicated by the black squares, are -27.1dBV, -26.9dBV, -25.6dBV and -24.2dBV for voltage gains of 83.8dB, 66.1dB, 38.1dB and 29dB respectively.

The IIP3 for voltage gain of 83.8dB is -27.1dBV. This is almost the worst IIP3 that the receiver can achieve because of the large voltage gain. There is still around 5dB margin between this value and the specification. The maximum deviation in the IIP3 for different gains is only 3dB. This implies that IIP3 is almost independent of the voltage gain of the VGA because, with the help of the out-of-channel attenuation of the mixer and filter, the IIP3 is mainly limited by the LNA and mixer.

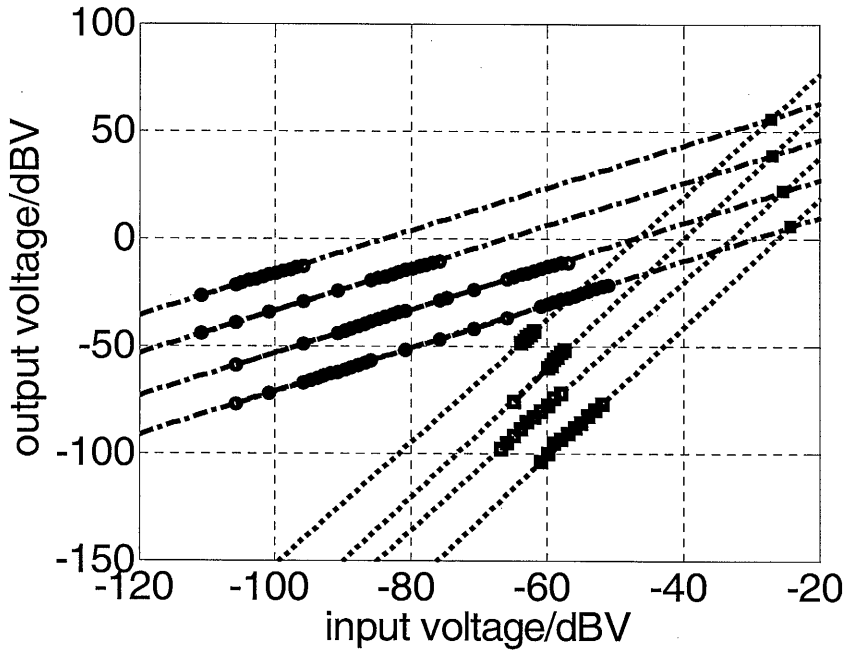


Fig. 7.14 Linearity of the receiver with different voltage gain

7.3.4.2 1-dB compression point

As mentioned in Chapter 3, the 1-dB compression point requirement is the input power with the addition of the PAPR. The requirement is the toughest when the input power to the receiver is the largest. Under such scenario, the conversion gain of the

receiver should be adjusted to the smallest value. In this measurement, the receiver is set to have the smallest voltage gain by turning off the negative gm cell in the LNA and reducing the gain of the VGA to the minimum. The measurement result is shown in Fig. 7.15. It shows a 1dB compression point of -33dBV, which meets the specified value.

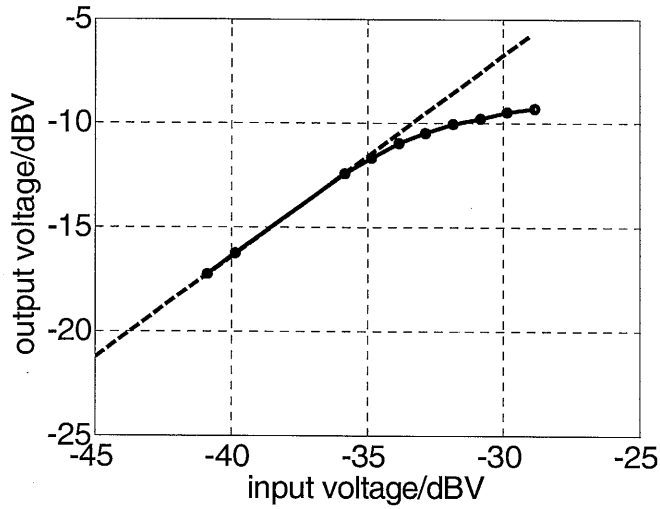


Fig. 7.15 Linearity of the receiver with the minimum conversion gain

7.3.5 Noise figure

In order to calculate the output noise density, it is inevitable to include the contribution from the loss from the cable, hybrid coupler and the microwave probes, both in the input and output of the receiver, as illustrated in the setup shown in Fig. 7.16. The power loss due to these components is represented as L_{in} and L_{out}.

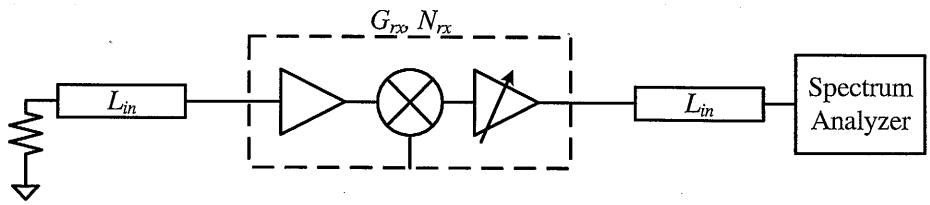


Fig. 7.16 Setup for the measurement of noise figure

The conversion gain and noise figure of the receiver alone is represented as G_{rx} and NF_{rx}. The equation for the total noise figure is written below in order to cancel out the contribution from L_{in} and L_{out},

$$\begin{aligned} NF_{tot} &= L_{in} + \frac{(N_{rx}-1)}{1/L_{in}} + \frac{(L_{out}-1)}{(G_{rx}/L_{in})} \\ NF_{tot} &\approx L_{in} + \frac{(N_{rx}-1)}{1/L_{in}} \quad if\ G_{rx} >> L_{in} >> L_{out} \\ \Rightarrow & \frac{n_{total,out}}{G_{total}} \frac{1}{kT} \approx L_{in} N_{rx} \\ \Rightarrow N_{rx} &\approx \frac{1}{L_{in}} \frac{n_{total,out}}{G_{total}} \frac{1}{kT} \\ \Rightarrow N_{rx} &\approx n_{total,out} - G_{total} - L_{in} - 174 dBm/Hz \end{aligned} \tag{7.2}$$

From the above equations, it is interesting to note that the loss at the output of the receiver can be ignored because its noise contribution is negligible owing to the large amount of conversion gain of the receiver. By using the above equation, the lowest noise figure of the receiver achieved is measured to be 8dB within the specified bandwidth. There is still a margin of 2dB from the target value.

7.3.6 SNR

The output signal-to-noise ratio of the receiver is the ratio of the desired output signal power to the total output noise power. It can be written mathematically as,

$$SNR_{out} = P_{out} - n_{out} - 10\log BW \tag{7.3}$$

where P_{out} is the output signal power and n_{out} is the output noise power density

The occupied bandwidth in IEEE 802.11a is 16.6MHz. Thus, the above equation can be re-written as,

$$SNR_{out} = P_{out} - n_{out} - 10\log 16.6M = P_{out} - n_{out} - 72.2dB \tag{7.4}$$

By injecting a sinusoidal tone within a channel, the ratio between the output signal power to the noise power density can be read directly from the spectrum analyzer.

Input attenuator of the spectrum analyzer is set to be the minimum allowable to ensure that the spectrum analyzer noise floor does not limit the noise floor to be measured. Noise marker is then used to measure the difference between the signal power and the noise power for a 1Hz noise bandwidth. The value prompted using the noise marker is then substituted into the above equation for calculation of the signal-to-noise ratio.

A signal power of -72dBm is applied at the input of the LNA. The received signal spectrum at the output of the VGA is shown in Fig. 7.16. The output SNR measured is, hence, 25.4dB. This is around 6dB larger than the specified output SNR.

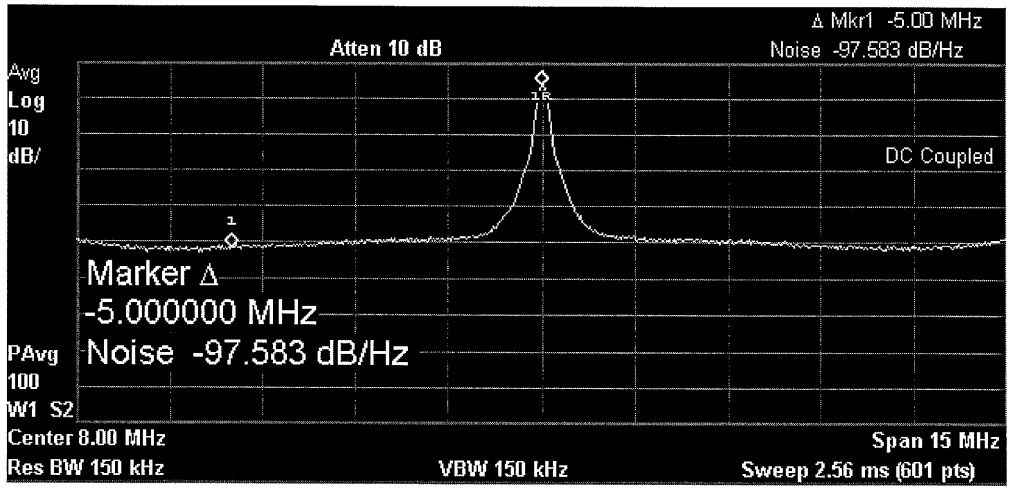


Fig. 7.17 Measurement result of output SNR

The output SNR with the same input power is measured at the other stages of the receiver. The measurement result is summarized in the level diagram shown in

Fig. 7.18. Thus, the sensitivity of the receiver is -72dBm with an output SNR of 25.4dB for a data rate of 54Mb/s in the IEEE 802.11a standard.

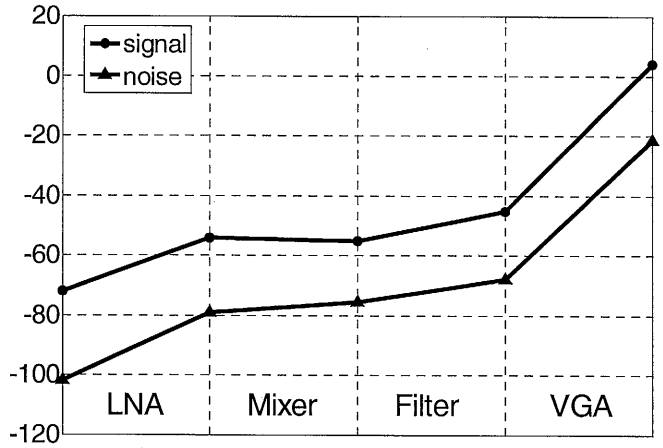


Fig. 7.18 Signal-level diagram of the receiver

7.3.7 DC offset

The mismatch of the DC bias at the outputs of the receiver is measured when the VGA is set to be at its maximum gain. The DC voltages of the quadrature channels of the receiver measured are summarized in Table 7.2. The average DC voltage is 0.738V. This is close to the expected DC bias, which is 0.75V. The maximum mismatch is 4mV, which is only 0.5% of the average value.

	I+	I-	Q+	Q-
DC	0.736	0.740	0.738	0.737

Table 7.2 DC voltages of the quadrature channels of the receiver

7.3.8 IQ imbalance

The amplitude and phase imbalance of the receiver are obtained using a network analyzer, as shown in Fig. 7.19. Due to frequency conversion existing in a receiver, the network analyzer, *Agilent 8753ES*, has to be operated under the *frequency offset mode* for the measurement. Port 1 of the network analyzer is connected to the input of the receiver. The I channel of the receiver is connected to the reference (R)

channel as the reference signal for the amplitude and phase. Its Q channel is connected to Port 2, also known as the *reflect* or *A* channel. The amplitude and phase imbalance are then available by reading the amplitude and phase response of *A/R*.

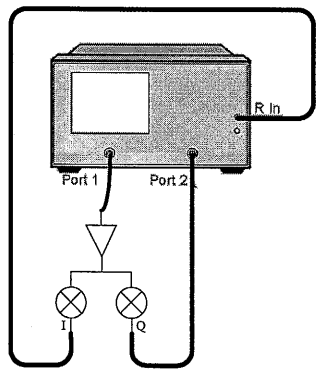


Fig. 7.19 Setup for measurement amplitude and phase imbalance using a network analyzer

The amplitude and phase imbalance measured are 0.17dB and 2.80°, as shown in Fig. 7.20. These values are well within the specification.

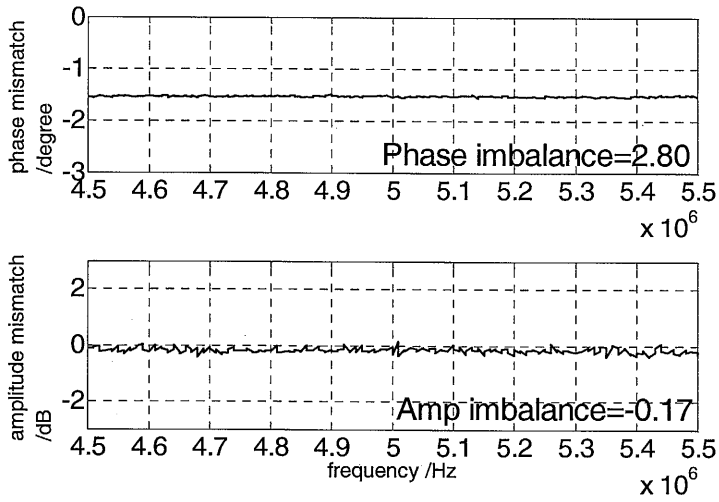


Fig. 7.20 IQ mismatch

7.3.9 ADC

The output spectrum of the quadrature ADC with a 1MHz signal is shown in Fig. 7.21. With a sampling rate of 40MS/s for each channel, the peak SNR, SNDR and SFDR of the ADC is 47.5dB, 44.4dB and 54.4dB respectively. With reference

voltages of 0.75V and 0.25V, the measured DNL and INL are +/-0.5LSBs and +/-1.1LSBs respectively.

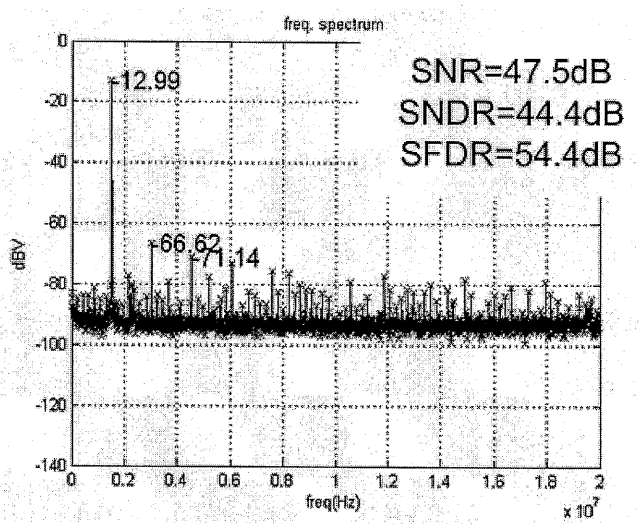


Fig. 7.21 Output spectrum of the ADC

7.4 Measurement results of the transmitter

7.4.1 DAC

The full-scale output current of the DAC is 1.5mA for a single channel. The SFDR remains above 50 dB up to an input frequency of 10MHz while the sampling frequency is fixed at 40MS/s. Its output spectrum is also shown in Fig. 7.22. The measured differential and integral linearity error are DNL=0.8 LSB and INL=0.8 LSB, respectively.

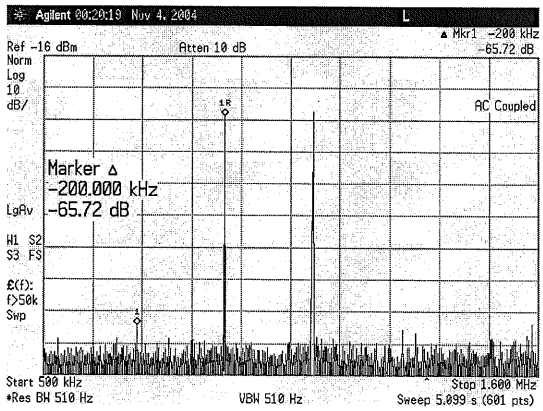


Fig. 7.22 Output spectrum of the DAC

7.4.2 Frequency response and conversion gain

The frequency response of transmitter is mainly determined by the band-pass characteristic of the transmission filter. A network analyzer is used to measure the S_{21} parameter at the output of the filter from 30kHz to 40MHz. Fig. 7.23 shows the measurement result of the conversion gain of the filter after calibrating out the loss from the cables and probes. The measured pass-band of the filter loss is 3.5dB. The lower and upper 3-dB frequencies are 98 KHz and 10.33 MHz respectively. The attenuation at 40MHz is 16.5dB.

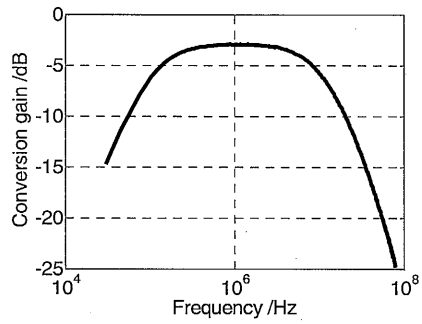


Fig. 7.23 Frequency response at the input of the transmission filter

The IQ imbalance of the filter is also measured. The mismatches are tabulated as shown in Table 7.3. The largest mismatch of the pass-band gain is 0.4dB which is the same as that for the attenuation at 40MHz. For the mismatches in the 3dB frequencies, the largest deviations are 0.3kHz and 0.106MHz for the lower and upper 3dB frequencies. This corresponds to less than 1% of the mean values.

Channel	Pass-band gain	Lower and upper 3dB frequencies	Attenuation @40MHz
I+	-3.71dB	108.4KHz, 10.865MHz	-16.3dB
I-	-3.51dB	108.1KHz, 10.9MHz	-16.6dB
Q+	-3.91dB	108.7KHz, 10.95MHz	-16.7dB
Q-	-3.71dB	108.7KHz, 10.844MHz	-16.4dB

Table 7.3 IQ mismatches of the transmission filter

Table 7.4 shows the conversion gain of all the stages in the transmitter. It is measured by applying sinusoidal signal at the input of the filter. The up-conversion

mixer is driven by LO signals generated by the on-chip frequency synthesizer. The total voltage gain is 5.3dB. With a 0.15Vpp signal from the DAC, the transmitter can generate an output power of -1dBm. This is around 1dB short from the specification.

Building block	Filter	Up-mixer	PA	Total
Measured voltage gain /dB	-3.5	4.5	4.3	5.3

Table 7.4 Voltage gain of all the stages in the transmitter

7.4.3 Linearity

The linearity of the transmitter is shown in Fig. 7.24. It is measured by applying 4 differential quadrature signals, generated by a vector signal generator, at the input of the mixer and measuring the transmitted signal at the output of the PA. The saturated output power of the transmitter is 0.3dBm. Its output-referred 1dB compression point is -1.3dBm.

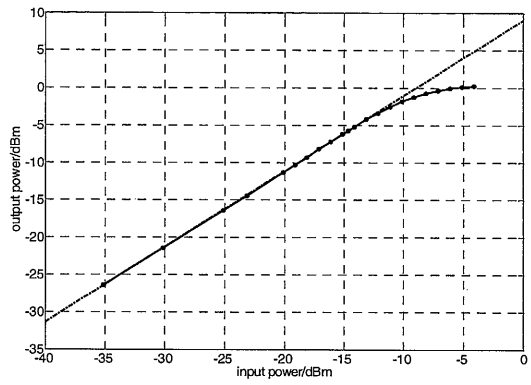


Fig. 7.24 1-dB compression point of the transmitter

7.4.4 LO leakage and sideband rejection

The sideband rejection and the LO leakage at the output of the PA is measured by applying a 5MHz sinusoidal signal, which is located at the center of the channel bandwidth, to the IF input of the up-conversion mixer. The LO signals applied are generated from the on-chip frequency synthesizer. The measurement result is shown

in Fig. 7.25. The measured LO leakage is 28.0dBc and the sideband rejection is 46.3dBc.

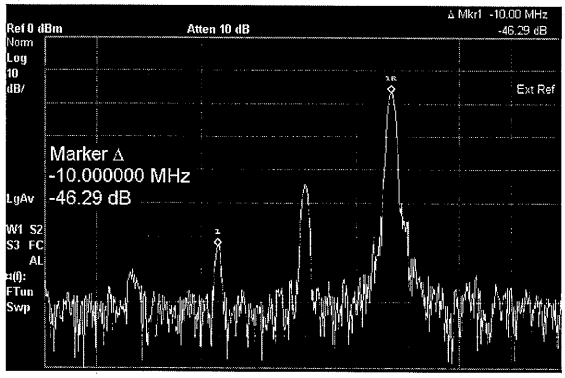


Fig. 7.25 LO leakage and side-band rejection of the transmitter

A contour plot relating sideband rejection, amplitude and phase mismatches is shown in Fig. 7.26. It shows that the measured sideband rejection of 46.3dBc implies a phase mismatch less than 0.5° and an amplitude mismatch less than 0.1dB in the IQ paths of the transmitter.

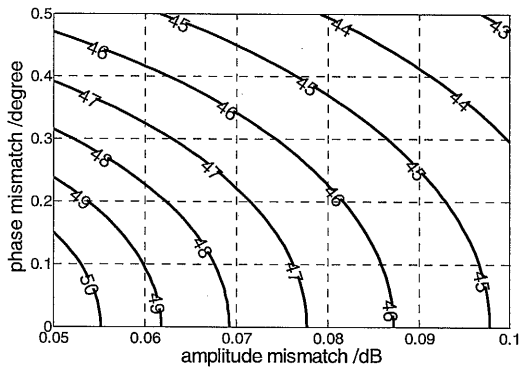


Fig. 7.26 Single-sideband rejection ratio versus amplitude and phase mismatches

7.4.5 EVM

Baseband OFDM packets with the modulation, 64-QAM, using a rate of 3/4, are created by the *Signal Studio 802.11a software* on a PC. They are then downloaded to the vector signal generator, which generates the corresponding analog quadrate differential signals for applying to the input of the transmitter. The OFDM signals is

then up-converted and transmitted at the output of the PA, which is connected to the input of the spectrum analyzer. The spectrum analyzer helps to down-convert the 5GHz OFDM spectrum and sends the down-converted signal to the vector signal analyzer. It detects and de-modulates the transmitted signal for WLAN modulation analysis. The workflow of the measurement is illustrated in Fig. 7.27.

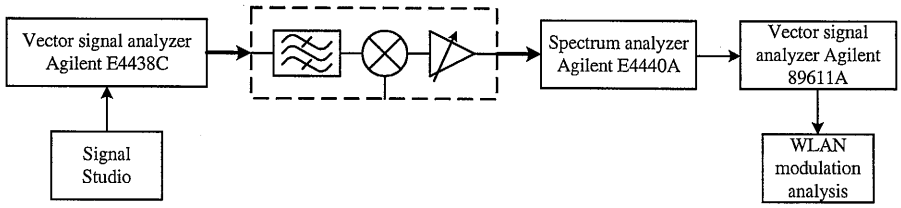


Fig. 7.27 Workflow for WLAN modulation analysis

With a power back-off of 10dB, the measured EVM is 4.5%rms or -27.7dB corresponding to an output power of -10dBm. By increasing the output power to -7.3dBm, the measured EVM increases to 5.5%rms. In IEEE 802.11a, an EVM of 5.6%rms is required for the 64-QAM modulation. Its measured output spectrum with the standard spectrum mask is shown in Fig. 7.28. The OFDM spectrum sent by the proposed transmitter is well under the spectrum mask specified in the standard. Fig. 7.29 shows the corresponding constellation diagram. The demodulated data in grey and the pilot in black are shown in the diagram.

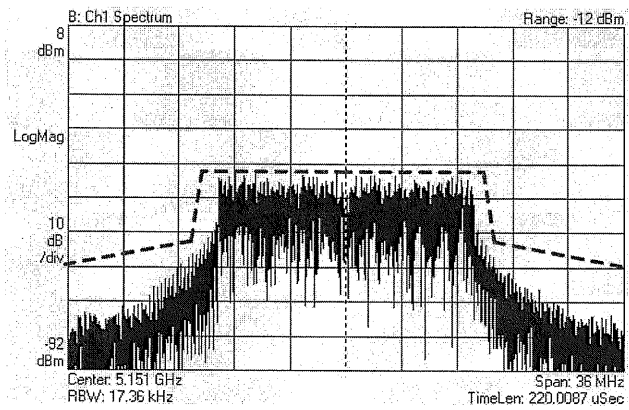


Fig. 7.28 TX output spectrum and spectrum mask

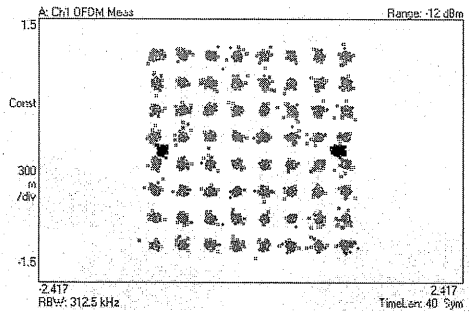


Fig. 7.29 Measured constellation diagram

The data demodulated and the modulation analysis done by the vector signal analyzer is displayed in the screen capture as shown in Fig. 7.30. It shows that the quadrature error and the gain imbalance of the transmitter under test are only 0.38° and 0.006dB respectively. These values comply well with the afore-mentioned sideband rejection, measured using a pure sinusoidal tone.

EVM	= -26.898	dB	EVM	= 4.5197	%rms
PilotEVM	= -28.486	dB	CPE	= 27.213	%rms
Freq Err	= 130.50	Hz	IQ Offset	= -22.059	dB
Quad Err	= 381.89	mdeg	Gain Imb	= -0.006	dB
Sync Corr	= 0.90341		SymClkErr	= -0.68	ppm
Mod Fmt	= 64QAM				
Octets	= 1024		Symbols	= 39	
Code Rate	= 3/4		Bit Rate	= 54.000	Mbps

0	00000000	01010100	01000001	00010001	01000001	01000100	0001 01
28	00000000	01010000	01000001	01000101	00000100	01010001	01172D37
56	162D013E	39302204	1F130939	1A012B0A	012E0D26	3B3F04	03083903
84	081D0126	22352109	1E330023	32082201	00320D0E	2E1C3C0A	313D0301
112	30141E1D	111E3716	23021631	10010107	3419262C	3C1C32	1C383601
140	2F372808	2C053A1A	0B3B1303	19001236	1B0C020F	0A120F0B	0112152C
168	101F302B	09151D19	070F0134	172D091B	21 1820	3B18041F	011E0139
196	35170336	3B3E3E33	3F0A0003	080F2928	35101934	1B00110C	3E26043C
224	29313611	23261300	373C0A05	203C 13	113E1311	1E001A16	231D0015
252	05182704	19263901	3C1C2F1B	2F032B27	0A2B002E	063D2E0B	15010417

Fig. 7.30 Modulation analysis results

An off-chip PA, *maxim 2841*, is connected to the output of the on-chip PA. Since the input of the off-chip PA is 50Ω terminated, a matching network is used in the interface of the on-chip and off-chip PA to ensure maximum power transfer. The above measurement is repeated with the off-chip PA. Fig. 7.31 shows the relationship between the output power and EVM of the proposed transmitter with and without the off-chip PA. In order to meet the specified EVM of 5.6%rms in the standard, the maximum output power allowable with the on-chip PA alone is

-7.3dBm. With the addition of the off-chip PA, the maximum allowable output power increases to 9.5dBm with a power back-off of 5.5dB.

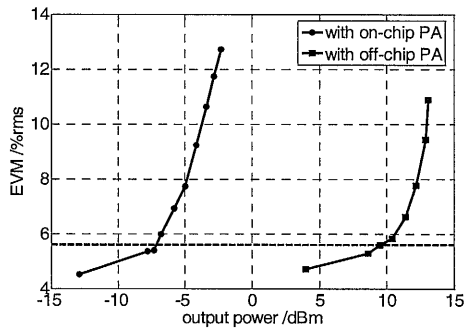


Fig. 7.31 EVM versus output power of the proposed transmitter

7.5 Performance summary of the transceiver

Implemented in 0.18-μm CMOS process, the total power consumption is 65.2 mW for the receiver and 32.7 mW for the transmitter. Table 7.5 shows the breakdown of the power consumption for each of the building blocks for the transceiver.

Building blocks	Power consumption /mW
Frequency synthesizer	
FS w/LO buffers	9.7
LO buffers	10.8
Total	*20.5*
Receiver	
LNA	11.7
Down-conversion mixer	9.8
Filter	4.7
VGA	9
ADC	30
Frequency synthesizer w/LO buffers	20.5
Total	*85.7*
Transmitter	
DAC	4
Tx-filter	0
Up-conversion mixer	13.8
PA	14.9
Frequency synthesizer w/LO buffers	20.5
Total	*53.2*

Table 7.5 Breakdown of the power consumption of each building block

All the measured performance of the transceiver is summarized in Table 7.6.

	Specification	Measurement
Receiver		
S_{11}	<10dB	<-13.4dB
Max voltage gain	34-86dB	14-94.5dB
Noise Fig.	<10dB	8.0dB
IIP3	>=-20dBm	-24.2dBV
1-dB cp (input-referred)	>=-24dBm	-33dBV
Sensitivity	<=-65dBm w/SNR=18.4dB	-72dBm w/SNR=25.6dB
IQ imbalance	0.4dB, 5°	0.17dB, 2.80°
Power consumption (including freq. synthesizer)	<100mW	85.7mW w/1V supply
Chip Area		1.1×5.2mm^2
Transmitter		
Output Power	>=0dBm	0.3dBm (Saturated output power)
1-dB cp (output-referred)	>=4.5dBm	-1.3dBm
EVM	<=5.6%	4.5%rms (Tx output=-10dBm)
Power consumption (including freq. synthesizer)	<100mW	53.2mW w/1V supply
Chip Area		1.1×4.2mm^2
Frequency synthesizer		
Tuning range	4.144-4.256	4.112-4.352GHz
Phase noise	<=-131.7dB@20MHz	-139.6dBc@20MHz
Power consumption (w/o LO buffers)	<10mW	9.7mW w/1V supply
Power consumption (w/LO buffers)	<30mW	20.5mW w/1V supply
Chip Area		1.1×1.3mm^2

Table 7.6 Performance summary of the proposed transceiver

Table 7.7 shows the table of comparison of the proposed transceiver with other designs. The proposed transceiver meets all the IEEE 802.11a specifications while achieving the highest integration level by integrating also the IQ ADCs and DACs. It also dissipates the lowest power with the lowest supply voltage while occupying the smallest chip area.

		I. Vassiliou, et.al.[49]	T. Maeda, et.al. [50]	This work
Process		CMOS 0.18μm	CMOS 0.18μm	CMOS 0.18μm
Supply Voltage		1.8V	1.8V	1V
Including IQ ADCs and DACs?		No	No	Yes
Power	RX + syn.	302mW	108mW	85.7mW
	TX+ syn.	248mW	118mW	53.2mW
	Synthesizer	N/A	N/A	9.7mW
Area		18.5mm^2	17.2 mm^2	12.5 mm^2
Max voltage gain		79dB	74dB	94.5dB
Sensitivity (for 54Mb/s)		-75dBm	N/A	-72dBm
RX NF (w/ max gain)		5.2dB	4.4dB	8dB
RX IIP3 (w/ min gain)		-8dBm	-2.1dBm	-11.2dBm
TX output P-1dB		6dBm	0dBm	-1.3dBm w/o ext. PA 15dBm w/ ext. PA
TX EVM (w/ power back-off)		-33dB (Pout= -5dBm)	N/A	-27.7dB w/o ext. PA (Pout=-10dBm) -25dB w/ ext. PA (Pout=9.5dBm)

Table 7.7 Table of comparison with other WLAN transceivers

Chapter 8 Conclusion

8.1 Problems encountered and proposed solutions

8.1.1 VCO

In the first version of the VCO with the stacked divider, the oscillation was dominated by the divider instead of the VCO itself. The oscillation of the VCO could not be adjusted even though the bias for the varactor had been changed. As a result, the output power was small and the phase noise was poor. In order to remedy this problem, the contribution to the oscillation from the VCO is increased much larger than the divider. This is achieved by resizing the VCO and divider transistors to increase the injected current driven into the stacked divider. In addition, the geometry of the transformer is changed to increase the coupling factor, *k*. A transformer with a 2-port Shibata coupler structure is used instead of the differential center-tapped topology. Its secondary coil is made of 2 single turn inductors connected together in parallel to maximize the edge coupling between the two coils, as shown in Fig. 8.1. The minimum spacing allowable in the process is used in order to increase the coupling between the coils.

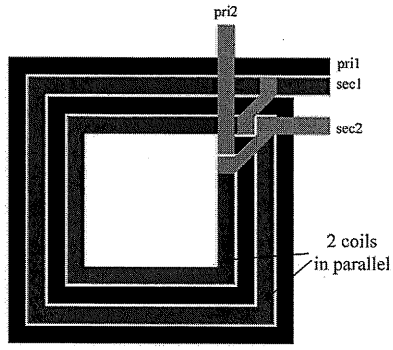


Fig. 8.1 Layout of the transformer with two parallel coils in the secondary coil

8.1.2 Transmission-line effect

At operation frequency of 5GHz, attenuation due to the transmission-line effect of the on-chip metal connection is no longer negligible. In the initial version of the transceiver, the LO signals driving the down-conversion and up-conversion mixers were attenuated much after traveling along the long metal connection in the layout. The gain of the transmitter also dropped significantly because of the long metal routing from the output of the up-conversion mixer to the input of the power amplifier.

This problem was solved by minimizing the length of such metal connections. Their width was also increased to reduce the parasitic inductance of the metal lines. The topmost metal was used to minimize the parasitic capacitance induced as a result of the increased width.

For those metal lines, which cannot be shortened, buffers are added to strengthen the high-frequency signals. Strong LO buffers are added at the output of the frequency synthesizer to drive both the down-conversion and up-conversion mixers.

8.1.3 Cross-coupling between metal connections

Cross-coupling between metal lines usually leads to signal corruption and ultimately entails in degradation of the overall performance of the whole circuit. This is especially significant in mixed-signal circuitry. For example, in the first version of the ADC, the metal connection for its sampling clock had many crossings with many parts of the circuit. The digital clock cross-coupled into the other metal connections and corrupted the internal signals. The cross-coupling accumulated and deteriorated significantly when the signals reached the output of the ADC. The spurious free dynamic range, is therefore, significantly degraded.

The problem was overcome by cautious floorplan in the ADC and shielding of the metal connection for the sampling clock.

8.1.4 Unwanted parasitic oscillation

Parasitic oscillations were found in the first version of the transceiver. One of them occurred in the PA and the other one in the DAC. Cascode structure was only used in one of the two stages of the PA. Due to the insufficient reverse isolation, the PA oscillates at a frequency close to the desired operation frequency and degrades the overall performance of the PA. This is solved by using cascode structure in both stages of the PA.

The other parasitic oscillation took place at the output of the current-steering DAC. In the current cell, as shown in Fig. 8.2, the parasitic capacitance, C_1 and C_2, are parts of the inherent parasitics of the transistors, M1 and M2, and the parasitics generated by the cross-coupling of nodes A and B with other metal lines. These two parasitic capacitors, C_1 and C_2, form a negative gm cell with the transistor, M2. When a bondwire is connected to the pad at the gate of M2 for off-chip voltage bias, parasitic oscillation starts when the negative gm is sufficiently large. This is similar to operation principle of a Colpitts oscillator.

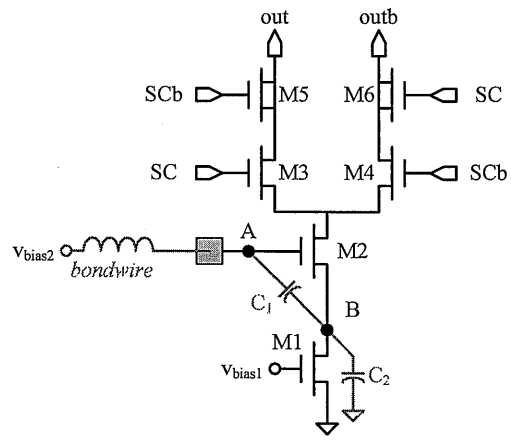


Fig. 8.2 Cause of the parasitic oscillation in the current cell of the DAC

Minimizing the parasitic capacitors at nodes A and B by reducing the length of the metal connections and their cross-coupling with other metal lines is one of the solutions. Another remedy is to add large on-chip bypass capacitors to the gate of M2. This helps to reduce the quality factor of the undesired LC tank formed after the connection of the bondwire. As a result, the negative gm formed by the parasitics and M2 is not large enough to start any oscillations.

8.2 Contributions of the dissertation

8.2.1 Novel design of a VCO and stacked divider

An ultra-low-voltage VCO using transformer feedback with a stacked frequency divider is proposed. The current flowing out of the divider is reused by the VCO, and the power can be reduced. In the measurement, the VCO can be tuned from 3.58-4.5GHz, corresponding to a tuning range of 920MHz (23%). The measured phase noise of the VCO is -140.5dBc/Hz at an offset of 20MHz with the carrier frequency being 4.36GHz. The power consumption of the VCO together with the first-stage divider is only 5.17mW under 1-V supply. Including the power consumed by the first-stage divider, its FOM is 180.14.

8.2.2 Design of an integer-N frequency synthesizer

An integer-N frequency synthesizer using the aforementioned VCO and stacked divider is proposed. The frequency tuning range of the frequency synthesizer is measured from 4.114-4.352GHz with a total number of 16 channels. The measured spur is -75.5dBc at an offset of 16MHz from the carrier frequency of 4.352GHz. The in-band phase noise at an offset of 10kHz is -71.1dBc/Hz and the out-of-band phase noise at an offset of 20MHz is -140.1dBc/Hz. Its power consumption is 9.7mW under 1-V supply.

8.2.3 Design and integration of an IEEE 802.11a transceiver

The system design and specification of the transceiver is proposed and derived. It uses a zero-IF, dual-conversion topology to eliminate the image-reject filter and relax problems with DC offset, *1/f* noise and LO self-mixing. The down-conversion and up-conversion mixers in the transceiver are successfully implemented. A single-chip IEEE 802.11a CMOS transceiver is then successfully implemented by integrating the mixers and the aforementioned integer-N frequency synthesizer with other building blocks contributed by members in the Analog Electronics Research Group in the Hong Kong University of Hong Kong, including Vincent Cheung, Gary Wong, Shuzuo Lou, Tay Hui, Rachael Wang, KaChun Kwok, Alan Ng, Dennis Lau and Patrick Wu.

The measurement of the transceiver is done. Its maximum voltage gain is 94.5dB with an out-of-channel IIP3 of -11.2dBm. The measured noise figure is 8dB. With a power back-off of 10dB, the measured EVM is 4.5%rms or -27.7dB corresponding to an output power of -10dBm. The total power consumption is 85.7mW for the receiver and 53.2mW for the transmitter, including the on-chip frequency synthesizer, under 1-V supply.

8.2.4 Novel design of a variable inductor and a dual-band VCO

Further development on the design of VCO is studied. An integrated variable inductor is proposed and analyzed. A dual-band VCO, employing such an integrated variable inductor, is demonstrated to oscillate from 2.2 GHz to 3.6GHz and 10.7 GHz to 11.3 GHz at a 1-V supply. The measured phase noise is around -118.2 dBc/Hz for the lower band and -110.0dBc/Hz for the upper band at 1-MHz offset while consuming 5mW. The corresponding FOMs are 182.7dB and 184.0dB. The

AAC of the proposed VCO is also demonstrated. The proposed VCO, can thus, be used to generate constant output power for the two different frequency bands.

8.3 Potential future work

8.3.1 Integration with baseband digital processor

The receiving path of the proposed transceiver starts from the LNA to the ADC and its transmitting path starts from the DAC to the PA. By connecting the proposed transceiver to a baseband digital processor, as shown in Fig. 8.3, a system-on-a-chip (SoC) that implements all the analog and digital PHY and MAC functions will be available. The baseband processor is recommended to be implemented under 1-V supply to take advantage of the low-voltage and low-power properties of the proposed transceiver. All the RF and mixed-signal operations are handled by the proposed transceiver. Thus, the baseband processor is only composed of digital circuitry, which should have no significant problem for operation under 1-V supply. Yet, careful floorplan is required to ensure that the digital circuitry does not affect the performance of the proposed transceiver.

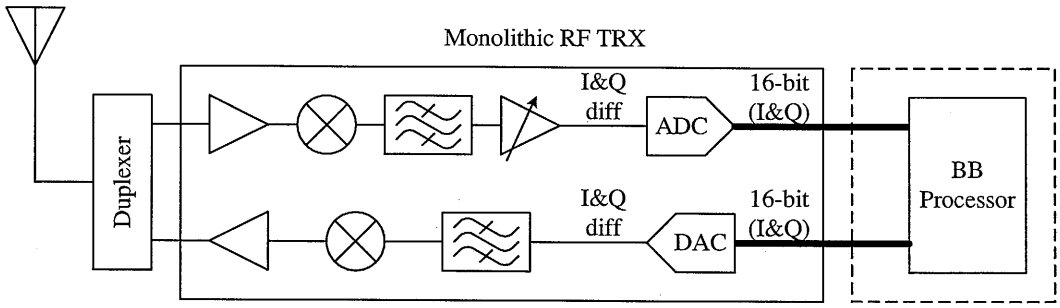


Fig. 8.3 Integration of the proposed transceiver with a digital baseband processor

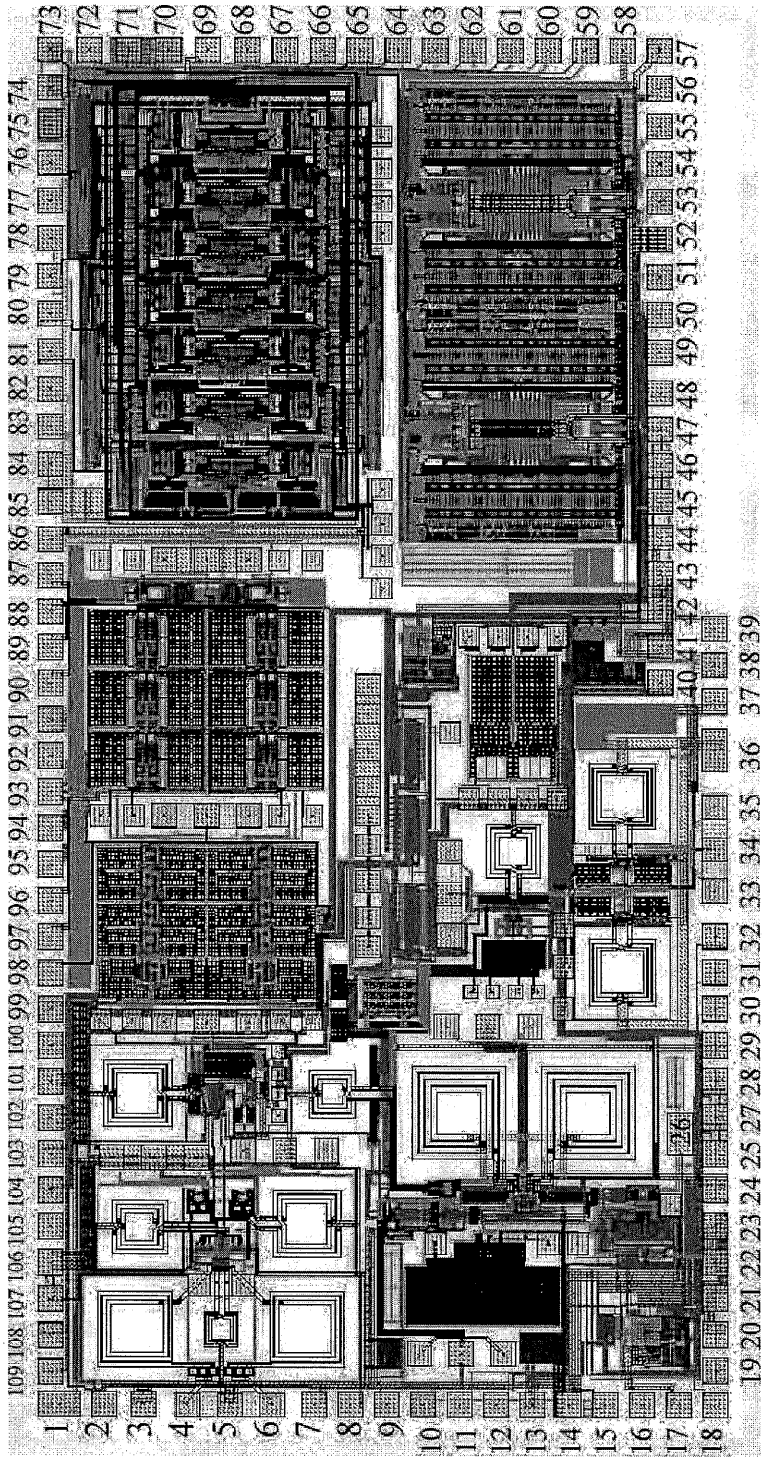
8.3.2 On-chip PA with high output power

For the time being, in order to generate high output power, an external PA is connected to the output of the proposed transceiver. In order to take advantage of the

SoC solution, another potential improvement is to integrate a linear PA with high output power onto the proposed transceiver. This on-chip enhancement requires special techniques to handle the tough output power and linearity requirement of the PA. High-performance passive components may be required. For example, the on-chip inductors need to have very high quality factor and the coils should have high current density to tolerate the peak current passing through them. The breakdown voltage of the transistors also has to be increased to handle the high output swing.

Appendix

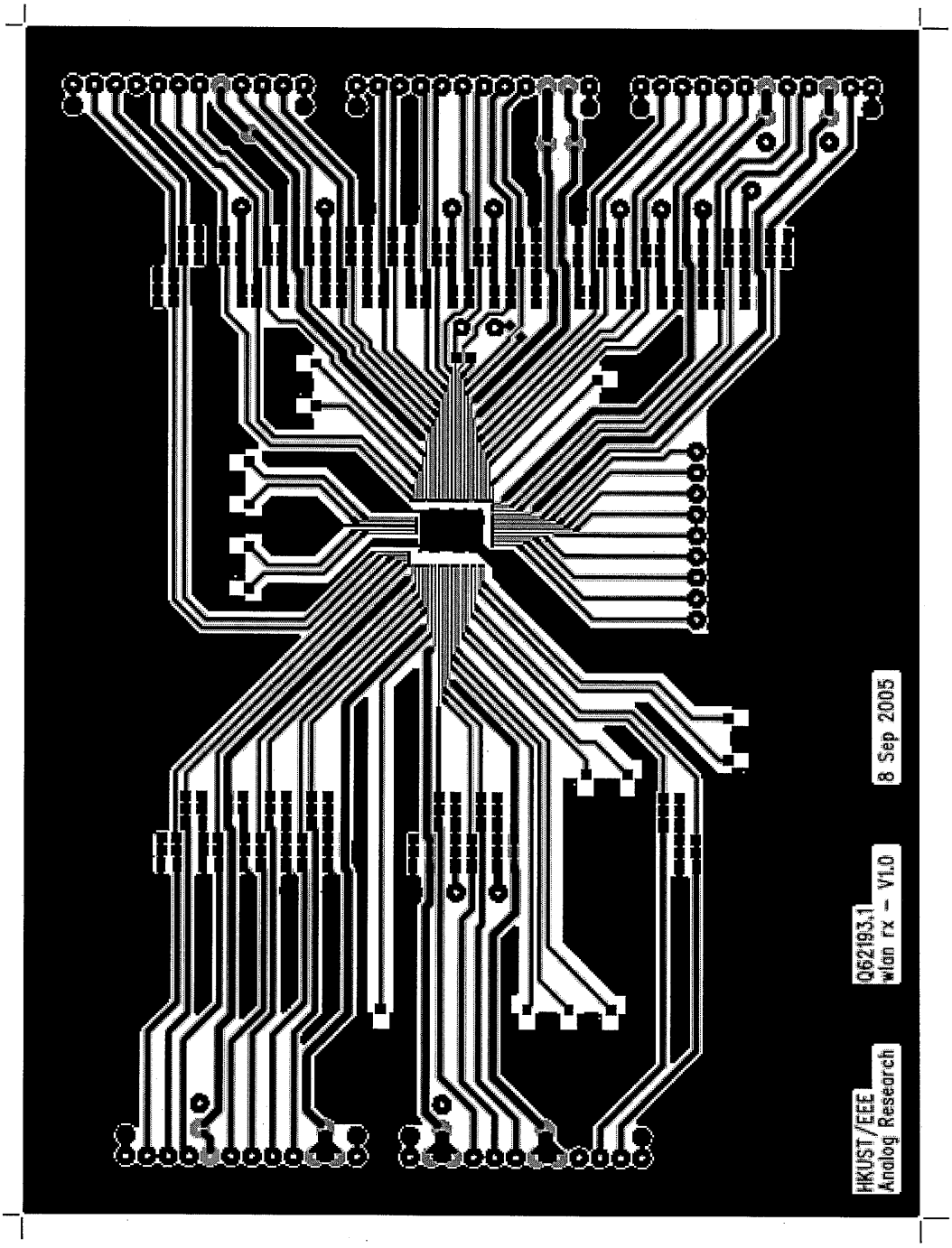
1. Layout of the proposed transceiver with pin numbers



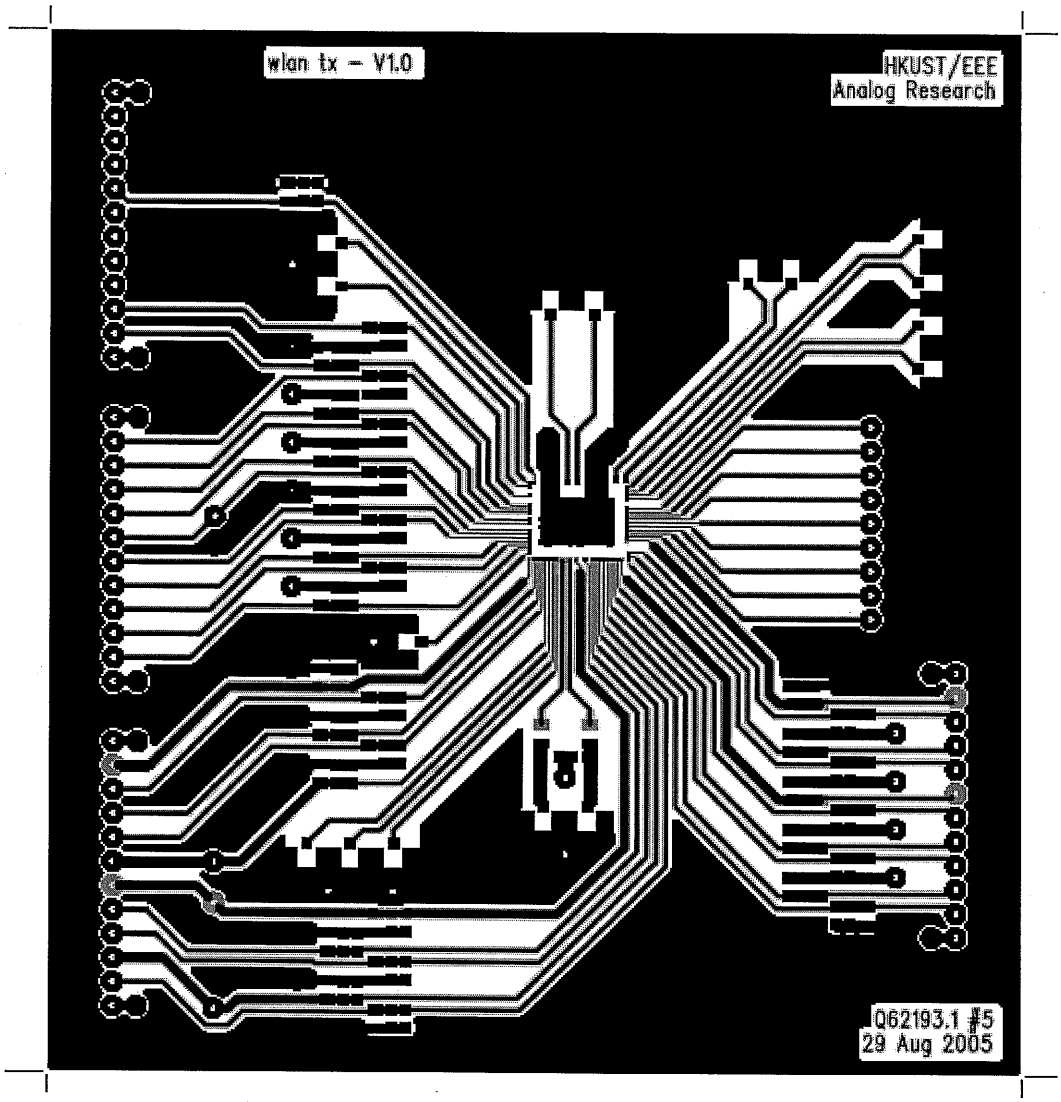
2. Pin Assignment

Pin No.	Pin Label	Type	Pin No.	Pin Label	Type	Pin No.	Pin Label	Type
1	Vdd_lo_fs	AVdd	38	Gnd_pa	SGnd	75	Vdd_clk_adc	DVdd
2	Vc_lna	V	39	Load_up	V	76	Mclk_adc	Din
3	Gnd_lna	Gnd	40	Gnd_up	AGnd	77	Gnd_adc	DSGnd
4	Inn_lna	Rfin	41	Gnd_bg	SGnd	78	Gnd_adc	SGnd
5	Gnd_lna	RfGnd	42	Inbias_up	V	79	B3_adc	V
6	Inp_lna	Rfin	43	Vdd_up	AVdd	80	B2_adc	V
7	Vdda_buf_fs	AVdd	44	Supply_bg	AVdd	81	B1_adc	V
8	Ext_bias_buf_fs	V	45	Vref_bg	V	82	Vrefp_adc	V
9	Ibias_buf_fs	V	46	Vbias_pa	V	83	Vrefn_adc	V
10	Gnd_fs	SGnd	47	Vlo_bias_up	V	84	Vdd_adc	AVdd
11	Cp_i2_fs	I_gnd	48	Bias1_up	I_vdd	85	Gnd_adc	AGnd
12	Cp_i1_fs	I_vdd	49	Bias2_up	I_gnd	86	SHD_vdd_adc	AVdd
13	Gnd_fs	AGnd	50	Vdd_dac	DVdd	87	RSSI_Q_vga	V
14	Vco_vdd_fs	AVdd	51	Vss_dac	DGnd	88	Vtune_vga	V
15	Div_Bias_fs	V	52	Vssa_dac	AGnd	89	RSSI_I_vga	V
16	Ext_bias_cp_fs	V	53	Vdda_dac	AVdd	90	Ext_ibias_vga	I
17	Supply_bg_fs	AVdd	54	Ibias_dac	I	91	Vdd_filter_vga	AVdd
18	Vref_fs	V	55	Vbias_dac	V	92	Gnd_filter_vga	SGnd
19	Gnd_fs	SGnd	56	Gnd_dac	SGnd	93	Gnd_filter_vga	AGnd
20	Vdda_Fs	AVdd	57	Vssd_dac	DGnd	94	Vc_I_vga	V
21	Gnd_fs	DGnd	58	Vddd_dac	DVdd	95	Vc_Q_vga	V
22	Ref_fs	V	59	D8	Din	96	Vr_vga	V
23	Vdd_fs (digital)	DVdd	60	D7	Din	97	Vcm_vga	V
24	Gnd_vco_fs	AGnd	61	D6	Din	98	Ext_ibias_filter	I
25	Gnd_fs	SGnd	62	D5	Din	99	Vbias_ext_dn	I
26	Neg_gm_bias_fs	V	63	D4	Din	100	Gnd_dn	SGnd
27	In_bias_3rd_fs	V	64	D3	Din	101	Vdd_dn	AVdd
28	In_bias_2nd_fs	V	65	Clk_dac	Din	102	Gnd_dn	AGnd
29	Vco_bias_fs	V	66	D2	Din	103	Vdd_sr	DVdd
30	Sr_in_fs	Din	67	D1	Din	104	Gnd_sr	DGnd
31	Sr_clk1_fs	Din	68	Gnd_adc	SGnd	105	Gnd_lna	SGnd
32	Sr_clk2_fs	Din	69	Vcbias_adc	V	106	Vdd_lna	AVdd
33	Voutn_pa	Rfout	70	Gnd_adc	DGnd	107	Ext_bias_lna	V
34	Gnd_pa	Rfgnd	71	Vdd_adc	DVdd	108	Sr_in	Din
35	Voutp_pa	Rfout	72	Gnd_adc	DGnd	109	Sr_clk1	Din
36	Vdd_pa	AVdd	73	Clk2ctrp_adc	Din			
37	Gnd_pa	AGnd	74	Clk1ctrp_adc	Din			

3. PCB for the receiving path in the proposed transceiver



4. PCB for the transmitting path in the proposed transceiver



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